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Final Report

POWER SUPPLY STANDARDIZATION AND OPTIMIZATION STUDY

July 1972

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TELEDYNE
BROWN ENGINEERING

Research Park • Huntsville, Alabama 35807

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FINAL REPORT
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POWER SUPPLY STANDARDIZATION AND OPTIMIZATION STUDY

By

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August 1972

Prepared For

ASTRIONICS LABORATORY
GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA

Contract No. NAS8-27798

Prepared By

SCIENCE AND ENGINEERING
TELEDYNE BROWN ENGINEERING
HUNTSVILLE, ALABAMA

ABSTRACT

This report describes a comprehensive design study of a power supply for use in the Space Shuttle and other space flight applications. The study established the design specifications for a power supply capable of supplying over 90 percent of the anticipated voltage requirements for future spacecraft avionics systems. Analyses and tradeoff studies were performed on several alternative design approaches to assure that the selected design would provide near optimum performance for the planned applications.

The selected design uses a dc-to-dc converter incorporating regenerative current feedback with a time-ratio controlled duty cycle to achieve high efficiency over a wide variation in input voltage and output loads. The packaging concept uses an expandable mainframe capable of accommodating up to six inverter/regulator modules with one common input filter module. The packaged configuration is designed to meet the EMI requirements of MIL-STD-461A, Amendment No. 3. Each inverter/regulator module will provide up to 50 watts of power at a selectable output voltage ranging from 4 to 108 volts. Pertinent characteristics and features of the power supply are

- Output voltage range -- from 4 to 108 volts
- Minimum efficiency -- 85% at 5 volts, 10 amperes
- Regulation line and load -- less than 0.02%
- Maximum temperature coefficient -- 0.005%/°C
- Maximum ripple -- 0.5% peak-to-peak
- Input-output voltage isolation -- to 1,500 volts
- Reverse voltage protection
- Programmable current limit
- Operation with total loss of input voltage -- 10 milliseconds
- Parallel operation
- Remote startup/shutdown capability
- Remote sense capability
- Overvoltage/undervoltage protection and monitoring.

Approved:

R. C. Ivy

R. C. Ivy, Manager
Electronic Systems Department

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August 23, 1972

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

DRA

Attention: Mr. Bert E. Johnson

Subject: Contract No. NAS8-27798

Gentlemen:

Enclosed please find the Final Report on the Power Supply Standardization and Optimization Study.

Contact the undersigned for additional information concerning this matter.

Very truly yours,

BROWN ENGINEERING COMPANY, INC.

Porter Gilbert

Porter Gilbert
Contract Manager

PG/hm

Enclosure

cc: DCAS/Mr. D. W. VanBrunt

1. INTRODUCTION

In the past few years, the many airborne and spaceborne avionics and control systems developed for aerospace vehicles have resulted in the almost universal acceptance of certain general requirements for airborne power supplies. It is logical to assume that these well-defined and accepted requirements could be incorporated into a standard design configuration for a universal power supply, or power conditioner, which could fulfill the needs of a high percentage of the power users in future aerospace programs. The Power Supply Standardization and Optimization Study was intended to provide a design for such a power supply. This final report presents the results of the study program.

The study was performed by the Electronics Systems Department of Teledyne Brown Engineering, under Contract NAS8-27798, for the Power Conversion and Regulation Section of the Power Branch, Astrionics Laboratory, of Marshall Space Flight Center. The study has resulted in the establishment of preliminary design requirements for an airborne power supply which will satisfy most of the needs of future manned space vehicles, and the development of a design for a power supply which fulfills those requirements.

Teledyne Brown Engineering wishes to express sincere appreciation to the members of the Astrionics Laboratory, Marshall Space Flight Center, as well as the employees of Teledyne Brown Engineering who provided encouragement and support during this study effort. In particular, we want to thank the following individuals for their contributions:

- R. Lanier and J. R. Graves, Astrionics Laboratory, Marshall Space Flight Center
- E. V. La Budde and G. S. Sandhu, Electronics Systems Department, Teledyne Brown Engineering.

2. OBJECTIVE AND ORGANIZATION

2.1 OBJECTIVE

The primary objective of the Power Supply Standardization and Optimization Study was to develop a design for a standard power supply for manned space vehicles, with special emphasis on the needs of the Space Shuttle and Manned Space Shuttle. The results of the study are documented in this final report.

2.2 ORGANIZATION

The study effort was divided into four phases to achieve the objective. These phases were:

- Phase I - Definition of the Requirements

  During Phase I, the requirements for conditioned power in the Space Shuttle and Manned Space Station were reviewed and analyzed. The information obtained from these reviews and analyses was supplemented with known performance characteristics for existing power supplies, and a preliminary design specification was prepared for the standard power supply. When necessary, tradeoff studies were performed to establish the best overall configuration for the supply.

- Phase II - Design Electrical Circuits

  The preliminary design specifications and the recomdations of the tradeoff studies performed in Phase I were used as the criteria for designing a power supply. In this phase, candidate circuits which were capable of providing the necessary performance, as defined in the preliminary design specification, were analyzed and a preferred design was developed.

- Phase III - Identification of Potential Hybrid Microcircuits

  The preferred circuit design for the power supply developed during Phase II was analyzed to determine those circuit functions which could be packaged as hybrid microcircuits. Preliminary specifications for each of the candidate circuits were prepared and submitted to hybrid vendors for review and pricing.

- Phase IV - Packaging

  The design for the power supply was packaged and documented. Assembly drawings were generated for several of the various components and sub-assemblies in the power supply. A thermal analysis of the package was performed to assure that excessive temperatures were not possible under worst case operating conditions.

The study organization is shown in more detail by the flow diagram in Figure 2-1.

The following sections of the report present a detailed description of the activities and accomplishments of each phase of the study.

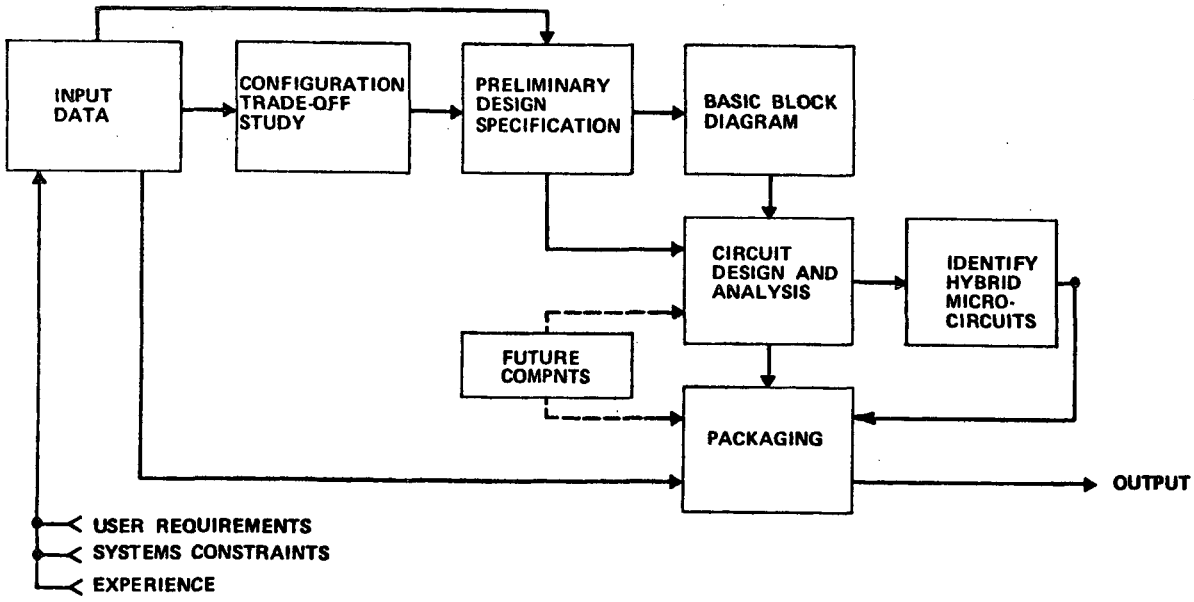

FIGURE 2-1. STUDY FLOW DIAGRAM

3. PHASE I ACTIVITIES AND ACCOMPLISHMENTS

As noted, the general objective of Phase I was to define the requirements for conditioned power in future space vehicles. In addition to this general objective, several more specific objectives were defined for this phase of the study. These were:

- Determine vehicle power system parameters which affect the power supply design
- Select an optimum overall configuration for the power supply
- Prepare a preliminary design specification for the power supply.

Each of these is discussed in detail in the following paragraphs.

3.1 DEFINITION OF REQUIREMENTS FOR CONDITIONED POWER

The general objective of Phase I, to define the user's requirements for conditioned power in future manned aerospace vehicles, was necessary to allow sizing of the various functional elements of the power supplies which must furnish such power. Also, the data provided by the power users were to aid in identifying special requirements that the power supply design must accommodate.

In Phase I of the study, a sequential, four-step approach was used in attempting to identify the power users and their requirements. The four steps were:

1. Contact cognizant personnel in the MSFC Astrionics Laboratory to identify potential sources of information.
2. Review all available reports and other documents on the Space Shuttle and Space Station.

3. Survey the power users identified in Steps 1 and 2 by mail to determine their requirements.

4. Follow up the survey by contacting the users by telephone and personal visits.

In Step 1, cognizant engineering personnel in the MSFC Astrionics Laboratory who were in a position to supply data on the Space Shuttle and Space Station were identified and contacted. Close liaison was maintained with the Conversion and Regulation Section of the Power Branch. As a result of these contacts, essentially all of the current documentation on the two programs was made available for review.

Step 2 of the effort consisted of a review of the documentation furnished in Step 1. The documents which were reviewed are shown in the references listed at the end of this report. A significant contribution from this review was the identification of many of the engineering personnel in the prime contractors' organizations who were responsible for preparing the requirements for the various subassemblies which would require conditioned power. Also, the documentation contained preliminary lists of the gross power requirements for the systems. These lists contributed significantly to the study effort in a manner which is discussed later in this section.

For Step 3, a power requirements survey form was prepared and distributed to key contractor personnel who had contributed significantly to the Phase B Shuttle study efforts. A total of 60 forms were mailed to persons at the following locations:

- McDonnell-Douglas Astronautics Company, Eastern Division
- North American Rockwell Corporation, Space Division
- TRW Systems Group.

The survey form was intended to identify

- The names of the various loads (black boxes, etc.) which require regulated power
- The total power required for each load
- The operating voltage levels utilized within the loads, and the percent of the total power utilized by each level
- Any special electrical requirements imposed by the loads which the power supply must provide
- The form factor, or shape, with which the power supply must comply.

As can be noted, most of these items are concerned primarily with sizing the power supply.

For Step 4 of the effort, several of the users were contacted by telephone to emphasize the purpose of the survey and to provide any assistance necessary for completing the form. In addition, a copy of the survey form was attached to a monthly progress report and mailed to persons at several cognizant governmental and contractor agencies.

Unfortunately, the survey to determine the users' requirements for power was not successful. The survey and the personal contacts resulted in very few (three) responses, which did not provide a sufficient basis for decisions on sizing the power supply, or for determining any special requirements. It is felt that the basic difficulty in obtaining these types of data resulted because the data required have not been generated at the time the survey was performed. At that time, the efforts on the Shuttle and the Space Station programs had been concentrated on gross sizing of the electrical system and definition of general requirements for power. Thus, information required for the effort under discussion here had not been defined. It should be noted that some of the data requested in the survey may not be available for some time to come.

In the absence of firm data from the power users, it was decided to establish requirements for the power supply design by utilizing the best available summary of possible future power demands; these appeared in a report prepared by McDonnell-Douglas Aerospace Corporation (Ref. 1). This report contained data on avionics complements for the Shuttle Booster and Orbiter Vehicles which identified the assemblies and a gross estimate of their individual power requirements. This information was reviewed and the various load power levels categorized into power ranges. These are shown in Table 3-1. As can be seen, most of the loads, which are identified as Line Replaceable Units (LRUs), require an input power level which lies between 10 watts and 150 watts. Based on these figures, the output power level for the standard power supply was established as being a range between 10 watts and 150 watts.

To complete the requirements, certain assumptions were made concerning the operating voltages required by the LRUs. These are shown in Table 3-2. They are based on previous experience gained by MSFC and Teledyne Brown Engineering from participation in many aerospace electronic programs and, to some extent, on the results of other recent power system studies.

Subsequent data on the avionics power loads for the Manned Space Station were available in a report issued by McDonnell-Douglas Aerospace Company (Ref. 2). The space station power data presented in this report were compatible with those shown in Table 3-1.

3.2 DEFINITION OF PERTINENT POWER SYSTEM PARAMETERS

It was necessary to define several characteristics of the power systems planned for future space vehicles to assure that the standard

TABLE 3-1. LRU POWER LEVELS

BOOSTER – 166 LRUs		ORBITER – 134 LRUs	
POWER RANGE	NO. OF LRU	POWER RANGE	NO. OF LRU
< 10 W	39 (NOTE 1)	< 10 W	15 (NOTE 1)
10 W TO 25 W	55	10 W TO 25 W	74
25 W TO 50 W	17	25 W TO 50 W	8
50 W TO 100 W	23	50 W TO 100 W	19
100 W TO 150 W	23	100 W TO 150 W	9
> 150 W	9 (NOTE 2)	> 150 W	9 (NOTE 2)

NOTES:

1. TRANSDUCERS (3 TYPES) AND GLIDE SLOPE RCVRs
2. COMPUTERS, MAINTENANCE RECORDERS AND SYMBOL GENERATORS

TABLE 3-2. ASSUMED LRU OPERATING VOLTAGES AND POWER LEVELS

VOLTAGES:	VOLTAGE NO. 1 = + 28 VDC VOLTAGE NO. 2 = + 15 VDC VOLTAGE NO. 3 = - 15 VDC VOLTAGE NO. 4 = + 5 VDC VOLTAGE NO. 5 = TBD VOLTAGE NO. 6 = TBD
POWER LEVELS:	VOLTAGE NO. 1 = 35% OF TOTAL VOLTAGE NO. 2 = 25% OF TOTAL VOLTAGE NO. 3 = 10% OF TOTAL VOLTAGE NO. 4 = 25% OF TOTAL VOLTAGES NO. 5 AND 6 = 5% OF TOTAL

power supply will interface properly and provide the desired performance. These are shown below with the applicable limits, or ranges, which may be experienced in the Shuttle and/or Space Station:

- The steady-state input voltage from the power system will be between 90 Vdc and 125 Vdc.
- Voltage transients on the input of the supply will not exceed those defined by MIL-STD-704A. Most of the transients to which the power supply will be exposed are expected to be much less severe than those specified by the military standard.
- The primary voltage source characteristics will be those of a large aerospace power system which uses solar array and batteries, fuel cells, or ac generators with a transformer-rectifier to provide the dc voltages.

The primary voltage level mentioned above is the voltage furnished to the power supply, at its input terminals, from the electrical distribution system of the vehicle. The range of the input voltage shown above was calculated by considering the tolerances on the primary power source voltages and the voltage drops caused by line resistances and switching and control devices. The calculations were made for the longest line in the Shuttle booster which was taken to be 74.5 meters (250 feet), or 149 loop meters (500 loop feet) of conductor.

Military Standard MIL-STD-704A has been used as a general guide for establishing the levels of transients which appear on the vehicle primary power system. It is emphasized that this standard was used only as a guide, since the quality of the primary power in future manned vehicles is expected to be considerably better than that defined in the standard. Of particular importance is the duration of time of a power interruption during which the power supply must furnish

regulated voltages to the loads. This duration has been assumed to be on the order of 5 to 10 milliseconds instead of 50 milliseconds to several seconds as defined in MIL-STD-704A.

The source characteristics, particularly the source impedances, have been defined as those of either solar array and electrochemical battery systems, fuel cells, or auxiliary power unit type ac generators which are used in conjunction with transformer-rectifier assemblies to provide dc voltage to the power supply.

3.3 SELECTION OF AN OPTIMUM CONFIGURATION FOR THE POWER SUPPLY

Several general configurations are possible for the power supplies which will be used in the complex multi-load power systems employed in large aerospace vehicles. For instance, one possibility is to have one very large, centrally located power supply which furnishes the necessary regulated voltages to all loads in a vehicle. Also possible is a large number of small power supplies; i.e., one for each load that requires regulated voltages for its operation.

During Phase I, a tradeoff study was performed to establish the optimum overall configuration for the power supply. Three candidate configurations were evaluated to determine the relative cost, weight, size, and electrical performance, and other characteristics of each when it is applied in the electrical power system of a large vehicle.

Guidelines for the study were established to give direction to the tradeoff analyses. These are:

- The power supplies must provide, or be compatible with, multi-redundant power systems such as the fail operational, fail operational, fail safe (FO/FO/FS), and fail operational, fail safe (FO/FS) concepts, regardless of the selected configuration of the supply.

- The loads which the power supplies service will be located in equipment racks which are positioned throughout the vehicle. Each load, or LRU, in a particular rack will require approximately the same power as the other loads in that rack.

- The primary input voltage to the power supply will be 120 Vdc.

The three power supply configurations which were evaluated are:

- Central power supplies, wherein four large, centrally located dc-dc power supplies, with multiple regulated outputs, supply regulated voltages to all LRUs throughout the vehicle

- Bay power supplies, wherein one medium power level supply, with a multiple regulated output, is located at each of the load centers (equipment bays). Each supply then furnishes regulated voltages to the LRUs in that bay

- Separate power supplies, wherein each LRU has a separate power supply which furnishes regulated voltages to it alone.

The results of the tradeoff study show that for large, multi-redundant power systems, such as those of the Shuttle and Space Station, a separate power supply for each identifiable load, or LRU, provides the optimum configuration. Again, it should be noted that the tradeoff parameters included cost, size, weight, electrical performance, reliability, maintainability, and several other factors.

The tradeoff study is documented in detail in Appendix B.

3.4 POWER SUPPLY DESIGN SPECIFICATIONS

The information compiled from the interim definition of the users' power requirements, the analysis of the interface constraints, and the results of the tradeoff study were used to prepare a preliminary

design specification for the power supply. The complete specification is shown in Appendix A. While the specification is preliminary, it does contain sufficient detail to be used to develop a circuit design for the power supply, which was the objective of Phase II of the study.

3.5 ACCOMPLISHMENTS

The accomplishments of Phase I of the study effort are:

- A set of requirements was established for conditioned power in the Space Shuttle. While these requirements do not represent the exact, detailed requirements for power in future space applications, they do form a sufficient base for sizing functional elements for a power supply for future space vehicles. Recently available data on the electrical power loads in the Manned Space Station are compatible with these requirements.

- The pertinent power system parameters and constraints which affect the design of an optimum power supply were defined.

- A tradeoff study was performed to determine the optimum overall configuration for the power supply. The results of the tradeoff study showed that a separate power supply for each of the definable loads (LRUs) would provide the best overall performance.

- A preliminary design specification was prepared for the power supply. The specification contains sufficient detail to allow circuits to be designed for the various functional elements of the power supply.

4. PHASE II ACTIVITIES AND ACCOMPLISHMENTS

The general objective of Phase II was to design a circuit for the power supply which would meet the performance requirements defined in Phase I. The first step in Phase II was to formulate a general approach to developing the optimum design. The approach selected was:

- Review the current airborne power supply technology, by means of a literature search, to establish a data baseline
- Generate a set of optimization guidelines to assist in performing tradeoff studies
- Review candidate block diagram configurations for the overall supply and generate a comprehensive block diagram of the selected optimum block configuration
- Develop a detailed power supply design, with supporting analyses.

4.1 REVIEW OF CURRENT AIRBORNE POWER SUPPLY TECHNOLOGY

A literature search was performed to review the current airborne power supply technology. The selection of reference data on current designs for high-performance, flight-quality power supplies was somewhat limited. The documents and designs reviewed are shown in the Bibliography of this report.

Configurations of designs reviewed were, for the most part, conventional. While most of the information gained was not directly applicable to the study effort, sufficient data was obtained to provide an insight into the present state of the art and establish a baseline for the performance factors which the new design should meet. The literature reviewed, which was of particular interest, included data

on several unique circuit designs, operating frequencies of power switching circuits in current designs, and some general ideas on hybrid packaging techniques. Although the information obtained in this step was not useful in selecting candidate arrangements, it was useful in tradeoff studies involving candidate circuits. These are discussed later.

4.2 OPTIMIZATION GUIDELINES

A number of study guidelines were established for the effort. These were intended to give some direction to the study and to provide a means of measuring the success of the effort. The guidelines are listed below.

- The selected power supply design must be suitable for uses in man-rated spacecraft
- The design must be readily adaptable to changes in load requirements
- Efficiency must be maximized to reduce heat dissipation
- The power supply must be maintainable using spares, tools, and test equipment available in large orbital vehicles
- The design must be cost-effective
- Size and weight must be minimum, consistent with the other guidelines
- A 1972 component technology base should be utilized if possible.

These criteria were used to select the optimum design from the candidates throughout the development of the design.

4.3 ANALYSIS AND SELECTION OF AN OPTIMUM OVERALL CIRCUIT CONFIGURATION

This portion of the study effort was devoted to developing and analyzing candidate configurations which could form the functional elements of the power supply design. The results of this effort led to the final selection of the optimum configuration, and the generation of a comprehensive block diagram.

4.3.1 Candidate Arrangements of the Overall Supply

4.3.1.1 Basic Block Diagram Selection - An analysis of the preliminary design specification (Appendix A) reveals that the design selected for the power supply must include two, and possibly three, basic functional elements. These are:

- Input filter and energy storage element
- Transformer coupled dc-to-ac inverter, or a dc-to-dc regulating inverter
- Output rectifiers, filters, and regulators (Regulators are needed if a conventional dc-to-ac inverter is selected for the design).

It should be noted that more than one of each of these functional elements may be required to implement a design which meets the specification. Also, other supporting elements such as over-voltage and over-current protection, remote shut-down circuits, etc., will be required. Only the base elements required for a regulated output are listed above.

Using the three basic functional elements, several power supply configurations were generated and analyzed so that an optimum configuration could be selected. The four basic arrangements developed and evaluated were:

Arrangement 1 - A configuration wherein a dc-to-ac inverter drives a relatively large power transformer which has multiple secondary windings, across which the output voltages are developed. An input filter and voltage regulators for each output voltage complete this configuration (see Figure 4-1).

Arrangement 2 - A configuration wherein each output voltage generated by the power supply has a separate dc-to-ac inverter which consists of switching elements and a transformer which has only those windings that are necessary to generate the particular output voltage. A separate voltage regulator for each output and a common input filter complete this configuration (see Figure 4-2).

Arrangement 3 - A configuration wherein one set of switching elements drives a separate power transformer for each output voltage. In this arrangement, all of the power transformers in a power supply will be driven by a common switching element. Each output voltage will require a separate voltage regulator, but a common input filter can be used for all outputs (see Figure 4-3).

Arrangement 4 - A configuration wherein a separate dc-to-ac inverter is used for each output voltage generated by the supply and the operation of the inverter is controlled such that its output voltage is regulated without using a separate voltage regulator circuit. Again, a common input filter is used for all outputs (see Figure 4-4).

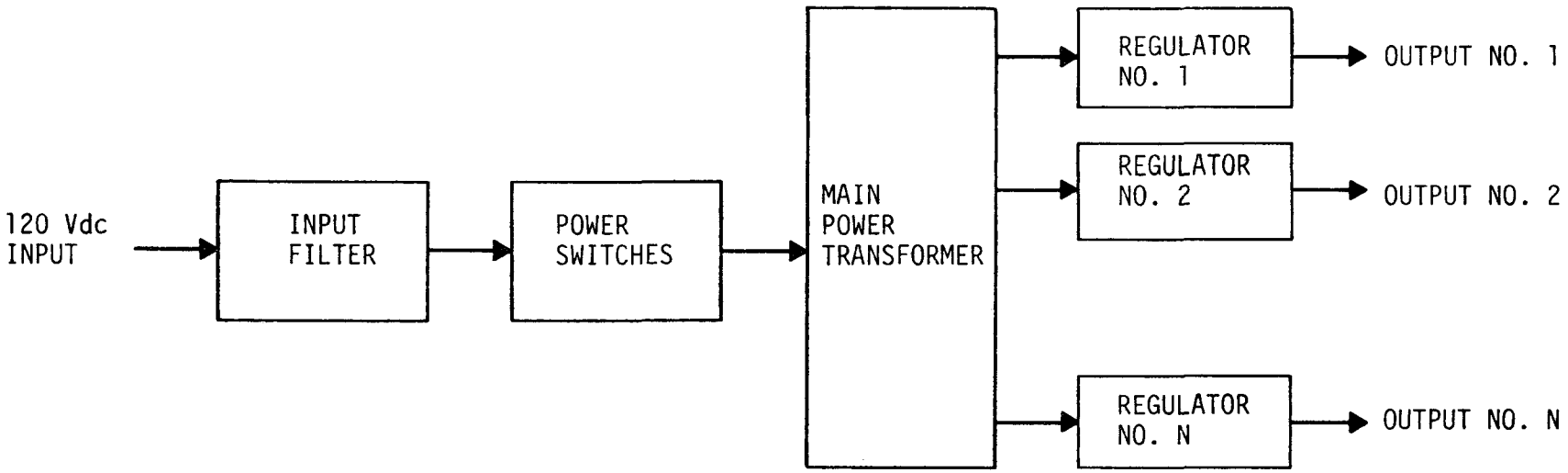

FIGURE 4-1. ARRANGEMENT NUMBER 1

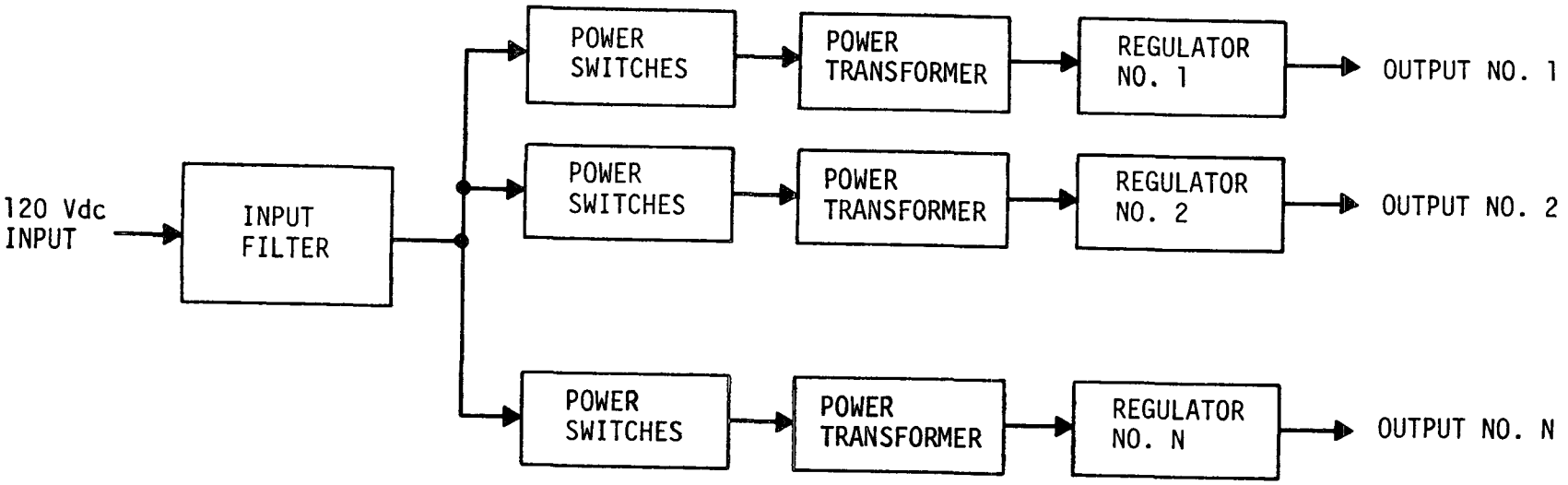

FIGURE 4-2. ARRANGEMENT NUMBER 2

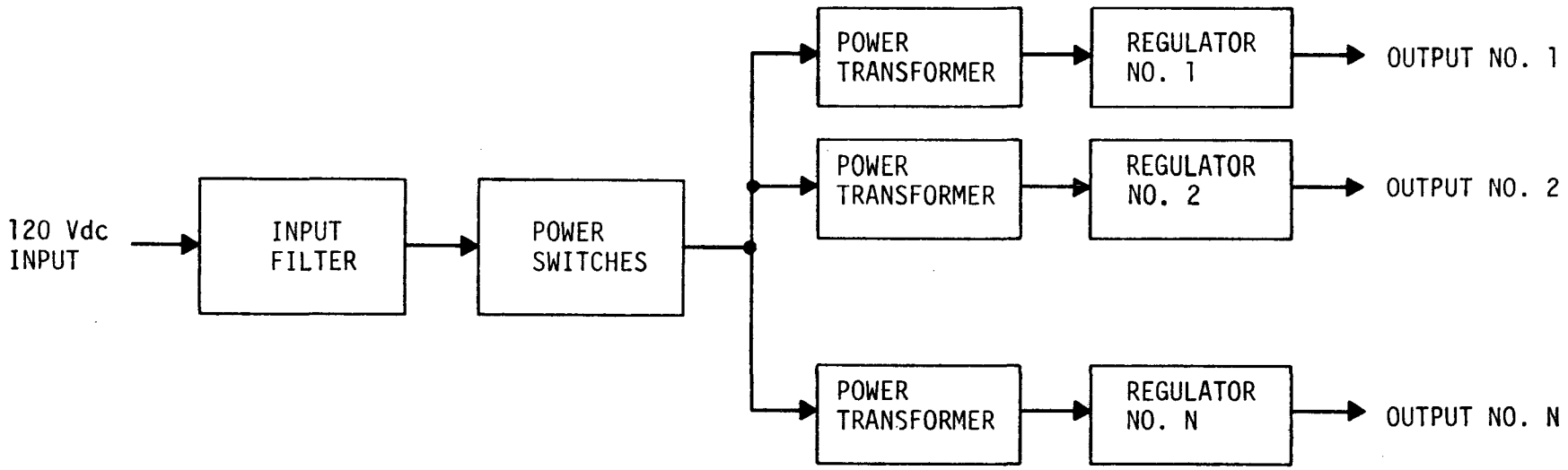

FIGURE 4-3. ARRANGEMENT NUMBER 3

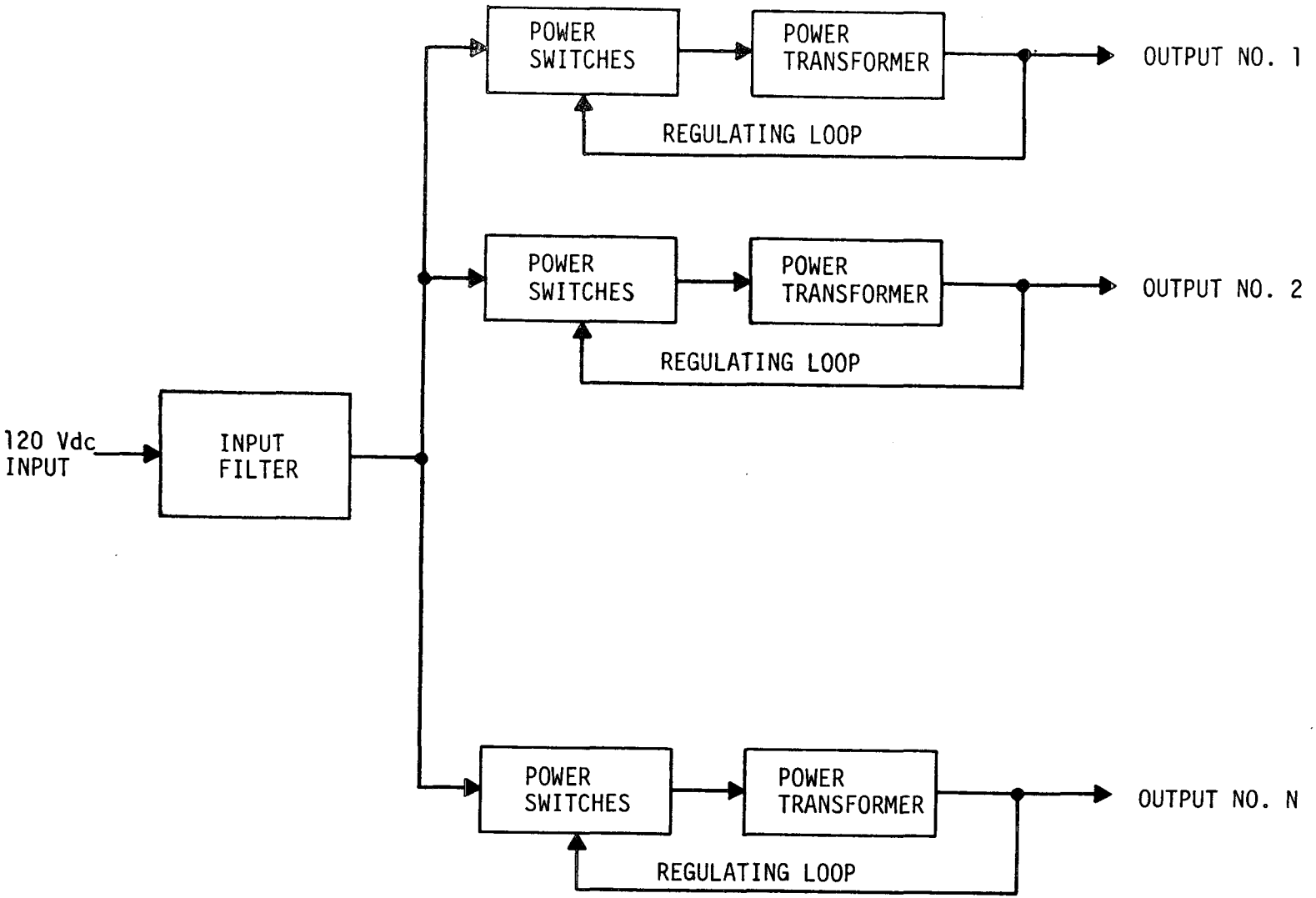

FIGURE 4-4. ARRANGEMENT NUMBER 4

There are advantages and disadvantages to each of the four arrangements if they are to be considered for use in the standard power supply. In the case of Arrangement Number 1, which is commonly used in existing airborne power supplies, the power transformer must be relatively large and complex, with many secondary windings. The failure of any one of these would require that the entire transformer be replaced, which would be costly. This arrangement is the least flexible and maintainable since a specific transformer design would be required for each load configuration, if the overall efficiency is to be optimized.

The second arrangement results in a much simpler transformer design, but it requires that a relatively large number of switching elements and a large amount of peripheral circuitry be used, thus complicating the package design and degrading reliability.

The third arrangement does not have any of the shortcomings of the first two, but it requires that some unusual design techniques be incorporated into both the transformer and switching circuits.

The fourth arrangement does not have the deficiencies of either the first or the third, since it utilizes multiple transformers in a non-parallel configuration. Also, since it does not require output regulators, it is somewhat simpler than the second. However, this arrangement is fairly complex.

The shortcomings of arrangements 1 and 2 were cause enough for them to be rejected as candidates for the design. It was not possible at this point to readily determine which of the latter two arrangements (arrangements 3 and 4) would best suit the required specifications for the standard power supply. Additional information as to their relative complexity, performance, and efficiency was required before such a determination could be made.

In order to ascertain this information, it was necessary to perform a more detailed analysis of these two possible candidate arrangements and develop a preliminary circuit configuration for each.

The two remaining candidate block arrangements selected for the power supply both consist of three basic elements: an input filter, a dc-to-ac inverter and rectifiers, and a voltage regulator, which may be an integral part of the inverter circuitry. Since a dc-to-ac inverter is common to both arrangements, it was selected as the first element to be analyzed in more detail to make a final selection for the configuration of the power supply.

4.3.1.2 Inverter Configuration Tradeoff Study - The approach for developing and analyzing the detailed circuit configuration for the inverter involved selecting the most effective and efficient means of generating the switching signal which drives the power transformer. An investigation into the selection of the configuration of the inverter required the analysis of several possible configurations. These were:

- A design wherein the main power transformer saturates and controls the switching frequency of the inverter (see Figure 4-5).
- A design wherein a saturating drive transformer is used to supply input current to the switching elements which drive a non-saturating output power transformer. An alternate arrangement of this particular configuration uses a saturating inductor in the input circuit to control the switching frequency (see Figure 4-6).
- A design wherein an input driving signal is transformer-coupled to the inputs of the switching elements through a non-saturated transformer. The switching elements then drive a non-saturating output power transformer (see Figure 4-7).

The first inverter circuit, while it is the least complicated, is not feasible for use in the parallel transformer design for the inverter, as required in candidate arrangement 3, since this arrangement

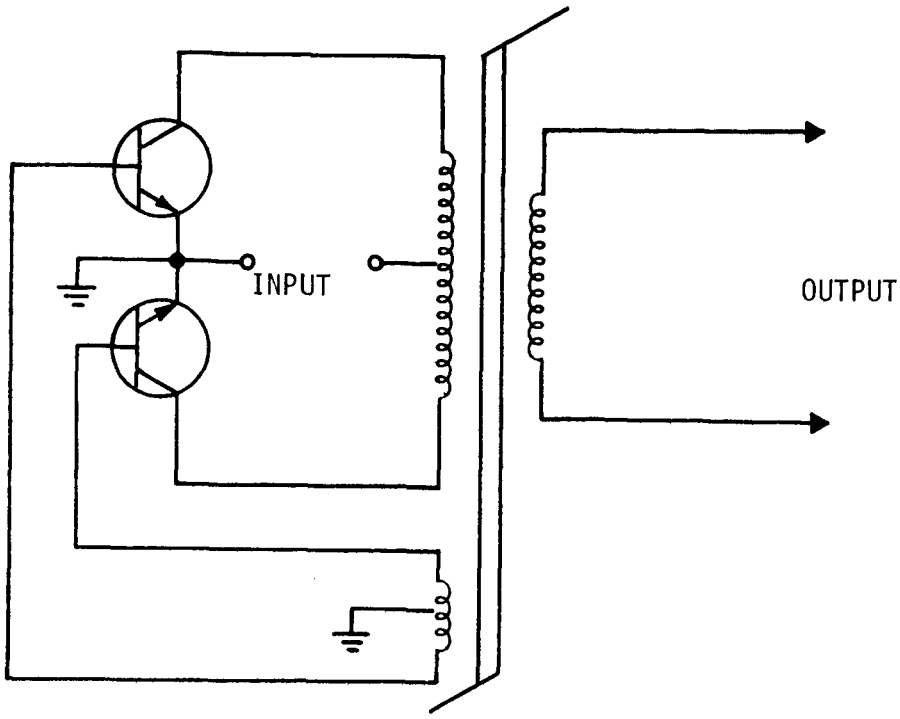

FIGURE 4-5. DC-TO-DC INVERTER WITH SATURATING OUTPUT TRANSFORMER

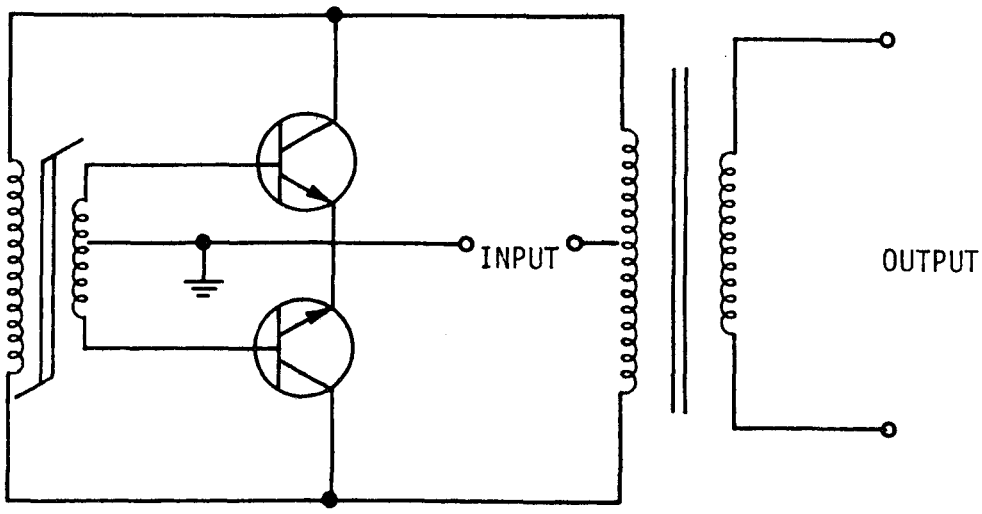

FIGURE 4-6. DC-TO-AC INVERTER WITH NON-SATURATING OUTPUT TRANSFORMER

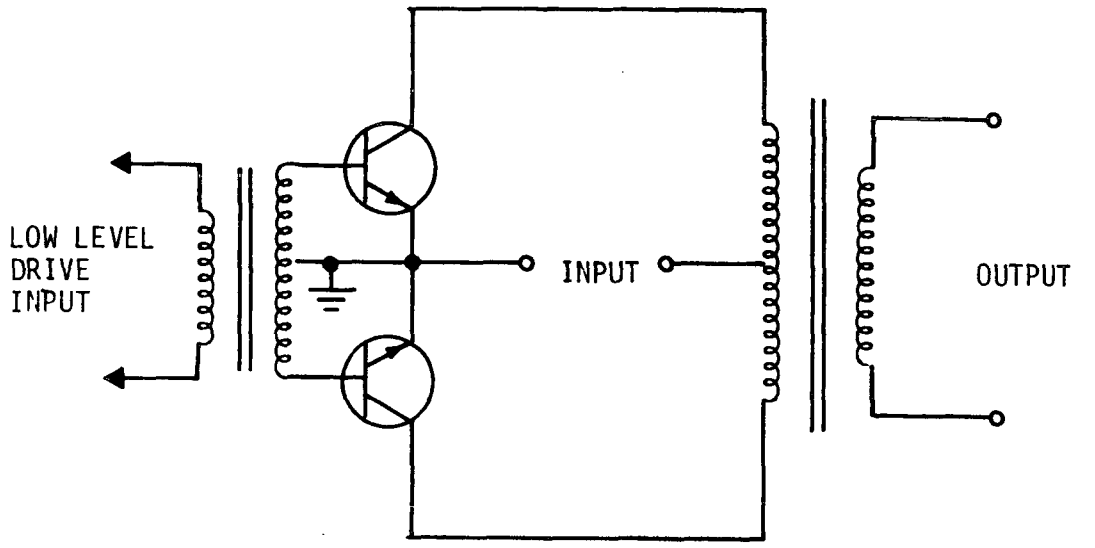

FIGURE 4-7. DRIVEN DC-TO-AC INVERTER WITH NON-SATURATING OUTPUT TRANSFORMER

requires that the drive signal be independent of the output power transformer. This circuit also exhibits a lower efficiency and higher electromagnetic interference (EMI) signal generation when compared to the other two candidate configurations.

Of the other two configurations, which are similar, the third has advantages in that it is slightly more efficient and the frequency of operation is determined by the low-level driving signal, so that it is independent of load variations and changes in the applied voltage. Also, on-off operation of the inverter in configuration 3 may be controlled by a simple logic function such as a NAND gate, which is used to inhibit the low-level driving signal. The third configuration, although it requires additional circuit complexity, was selected for use in the power supply. The detailed analyses of the three types of inverters are shown in Section C. 1 of Appendix C.

4.3.1.2.1 DC-to AC Inverter Input Considerations - The initial investigations in the problem of generating the waveforms in the dc-to-ac inverter indicated that maintaining high efficiency over a wide range of loads could be a basic problem. Analysis of several existing inverter designs revealed that one of the major causes of power loss in the circuits resulted from the use of "voltage drive" to supply input current to the switching elements, which are usually bi-polar transistors. In this technique the input current to the transistors is derived from a voltage source, which varies with changes in input voltage to the inverter circuit. Also, the magnitude of the drive current is sized to assure proper operation of the circuit when the maximum load power is supplied. As a result, excessive input current is supplied to the switches when the load is reduced below the maximum design value, and this produces an unnecessary power loss at relatively low output load values.

To overcome this undesirable condition in the design for the power supply, a technique for developing an input drive signal, identified as "current drive", was utilized. In this arrangement, the circuits which supply base drive current to the main switching elements were configured such that the input drive current to the switching transistors is proportional to the transistors' collector current which, in turn, is proportional to the load current. Although this design was somewhat more complicated than the voltage drive arrangement, it was selected for use in the power supply since it does result in more efficient operation of the inverter, particularly at light loads. A simplified schematic diagram of the design is shown in Figure 4-8, and a complete discussion of the technical aspects of the design is given in Section 4.4.5.

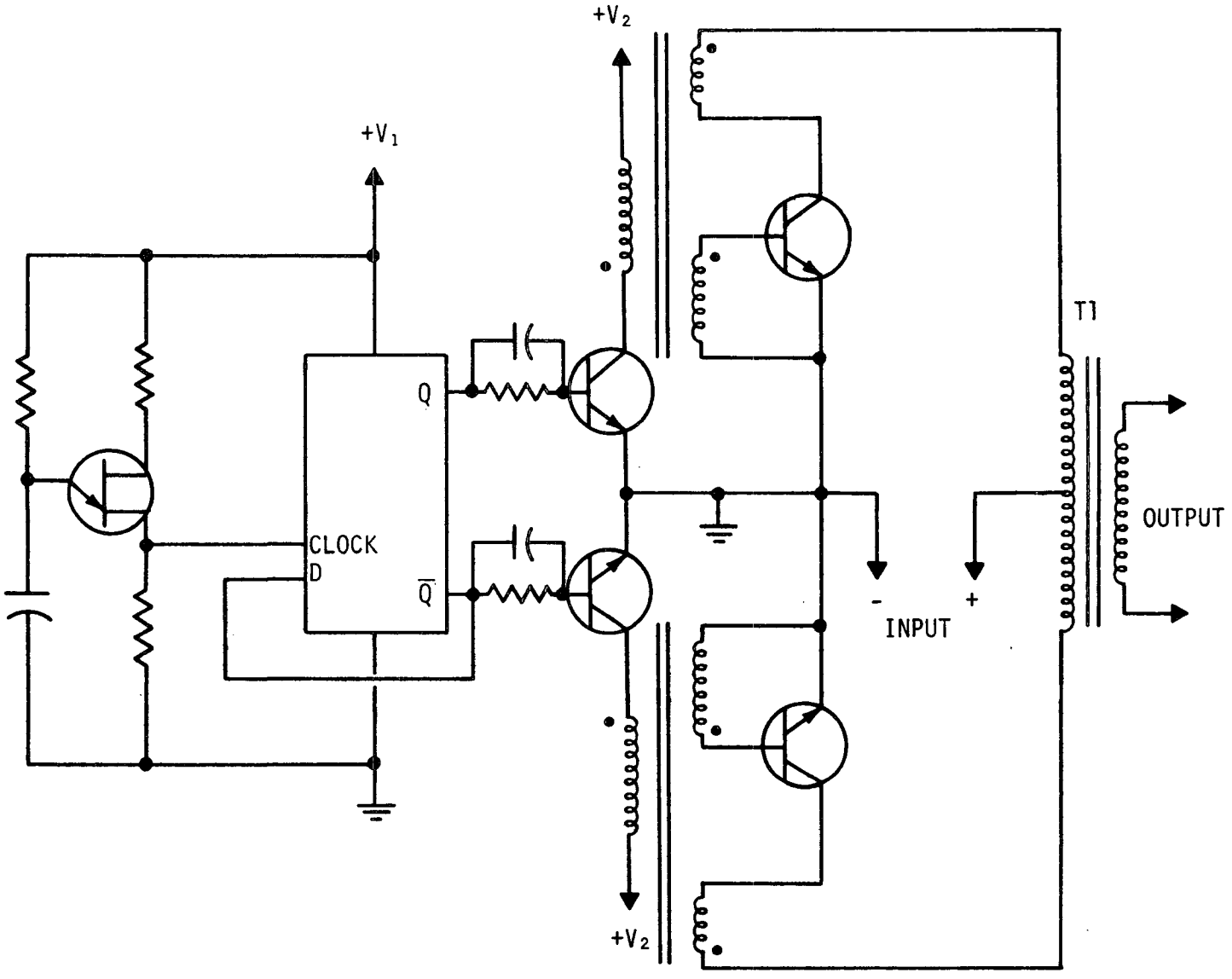

FIGURE 4-8. SIMPLIFIED DIAGRAM FOR DC-TO-AC INVERTER WHICH UTILIZES CURRENT MODE BASE DRIVE

4.3.1.2.2 Inverter Power Switch Configuration - Figure 4-8 shows the design for an inverter which utilizes two switching transistors in a "push-pull" configuration to drive the output transformer. This is a relatively standard arrangement which is commonly used in dc-to-ac inverters. However, it is possible to perform the switching function with only one transistor in a "single-ended" design. The latter type of a circuit appears to offer some advantage over the former since it would require fewer components and, therefore, would be more reliable and less expensive. To clearly establish which design (i.e., one switching transistor or two) should be used in the inverter circuits for the power supply, a tradeoff analysis which compared the two versions was performed. The conclusions of the tradeoff analysis are as follows:

- Peak transistor collector currents in the single-ended design are four times greater than those in the push-pull configuration. This requires that switching transistors with relatively high peak current ratings be used in the design. In general, such devices have lower current gain, higher saturation voltages, and slower switching times than lower current devices which could be used in the push-pull configuration and, as a result, the losses in the single-ended transistor are higher.

- The usable flux change, $\Delta\phi$, in the transformer in the push-pull design is 25 to 50 percent greater, for a given core size, than in the single-ended design. Thus, a smaller transformer can be used in the push-pull configuration.

The complete tradeoff analysis is shown in Section C.2 of Appendix C.

4.3.1.3 Output Voltage Regulators - One of the design configurations (arrangement 3) which was tentatively selected for the power supply had a separate voltage regulator for each of the output voltages. Several possible circuit configurations for voltage regulators were capable of providing the required voltage regulating capability in the power supply design. However, most of these had one or more inherent deficiencies which make them less than optimum for this application. A wide variety of basic regulator types were evaluated to select a design for use with arrangement 3. These candidates are:

- Series Types
  - ▲ Linear pass regulator
  - ▲ Switching regulator with series switch
  - ▲ Magnetic amplifier (saturating reactor) regulator
- Shunt Types
  - ▲ Linear regulator
  - ▲ Switching regulator with shunt switch
- Other
  - ▲ Ferroresonant transformer.

In the evaluation of these types, the series linear pass regulator, both of the shunt-type regulators, and the ferroresonant transformer were found to be unacceptable because they all are relatively inefficient.

To achieve an overall power supply efficiency of 85 percent, the regulators must exhibit individual efficiencies on the order of 90 percent or greater. Only the pulse width modulated (switching) regulator and the magnetic amplifier types are capable of achieving this level of efficiency. Of these two, the switching regulator has the advantage of lower size and

weight and better response times to load transients. Based on these advantages, the switching regulator was selected as the type to be used in Arrangement 3 of the power supply. Figure 4-9 shows a simplified schematic diagram of the regulator.

4.3.2 Discussion

The results of the analysis of candidate arrangements (Section 4.3.1), combined with the efforts to evaluate candidate circuits, enable a more detailed construction of the two remaining candidate arrangements, i.e., arrangements 3 and 4 (Section 4.3.1). These arrangements are shown in Figures 4-10 and 4-11.

An analysis of arrangement 3, which utilizes a dc-to-ac inverter that supplies power through multiple transformers to their corresponding output switching regulators, showed that substantial power losses were incurred in two component elements of each switching regulator. These two components were the main series switching transistor and the reverse recovery diode. If one or both of these elements could be eliminated from the circuit, the power losses could be greatly reduced.

The use of new components, i.e., Schottky diodes and high-speed switching transistors, results in reduced power losses. However, these losses are still substantial. Elimination of one or both of these sources of loss from the regulators would be highly desirable. The results of the analysis on these output voltage regulators are shown in Section C.3 of Appendix C.

Arrangement 4 provides a means whereby the recovery diode and series switching transistor can be deleted from the design without sacrificing any performance from the power supply. This technique

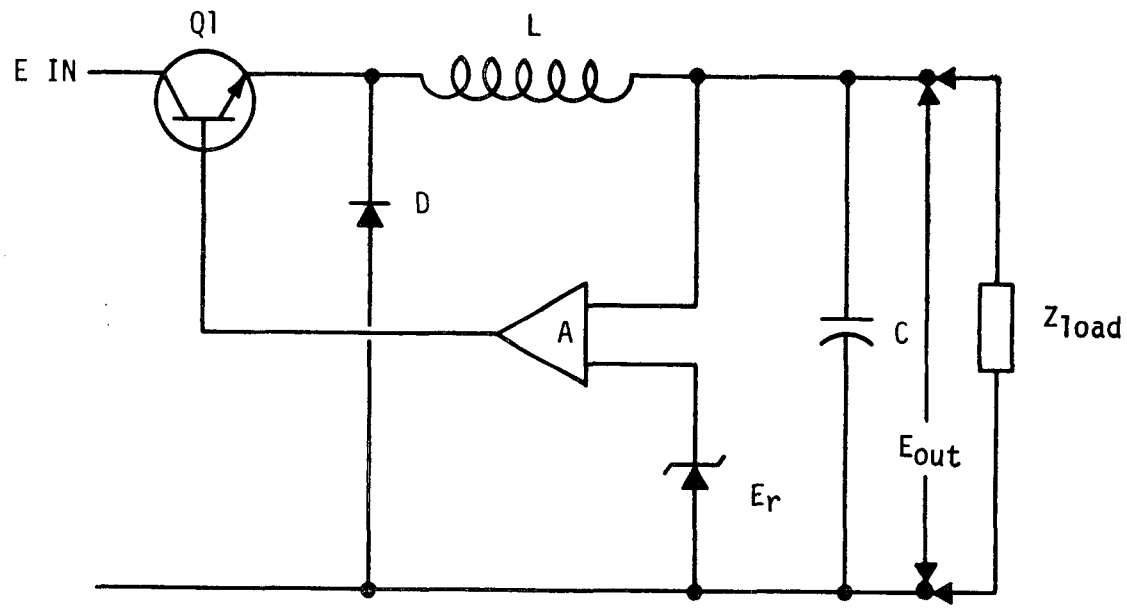

FIGURE 4-9. GENERAL SCHEMATIC OF SWITCHING REGULATOR

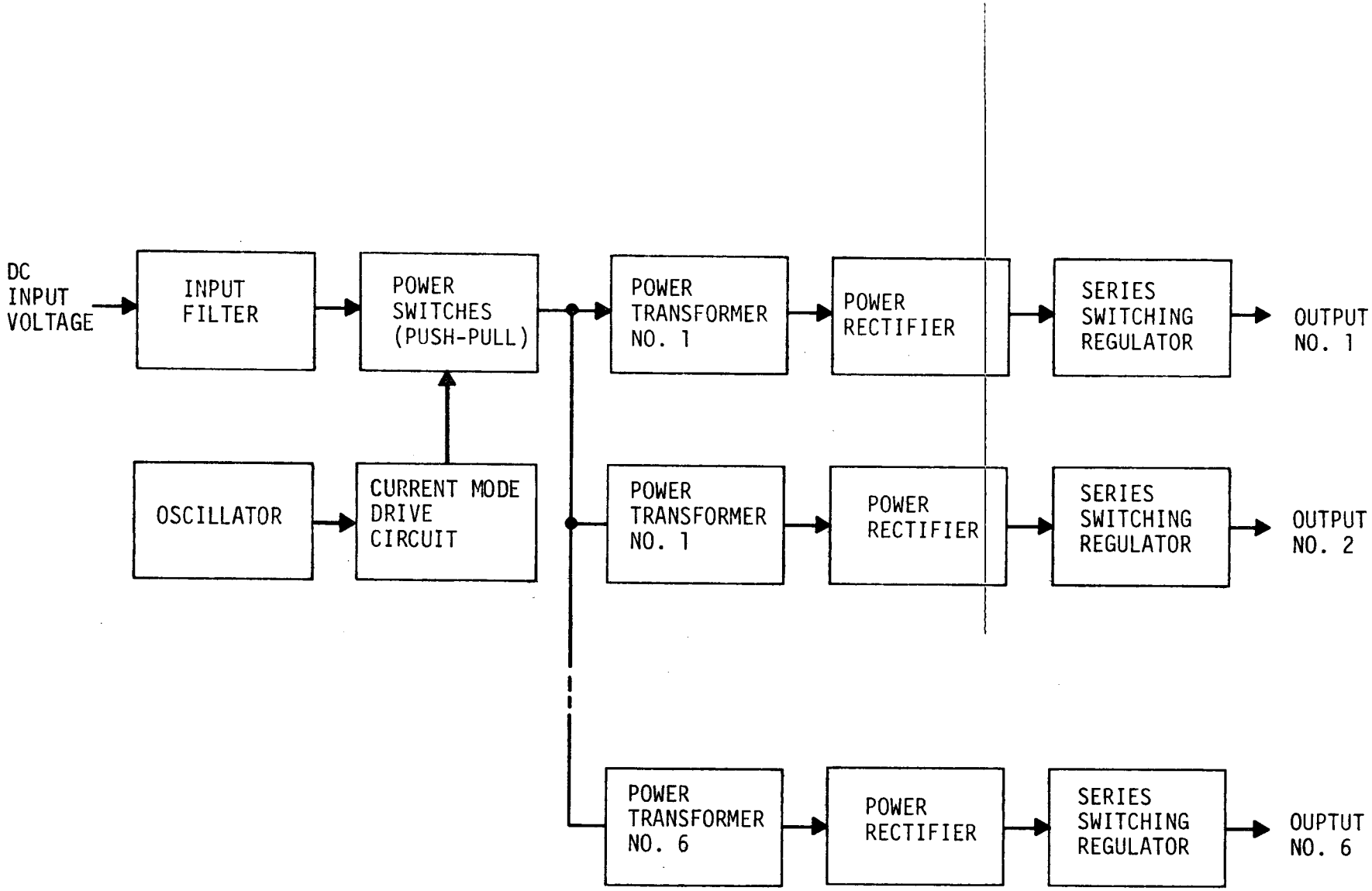

FIGURE 4-10. ARRANGEMENT 3

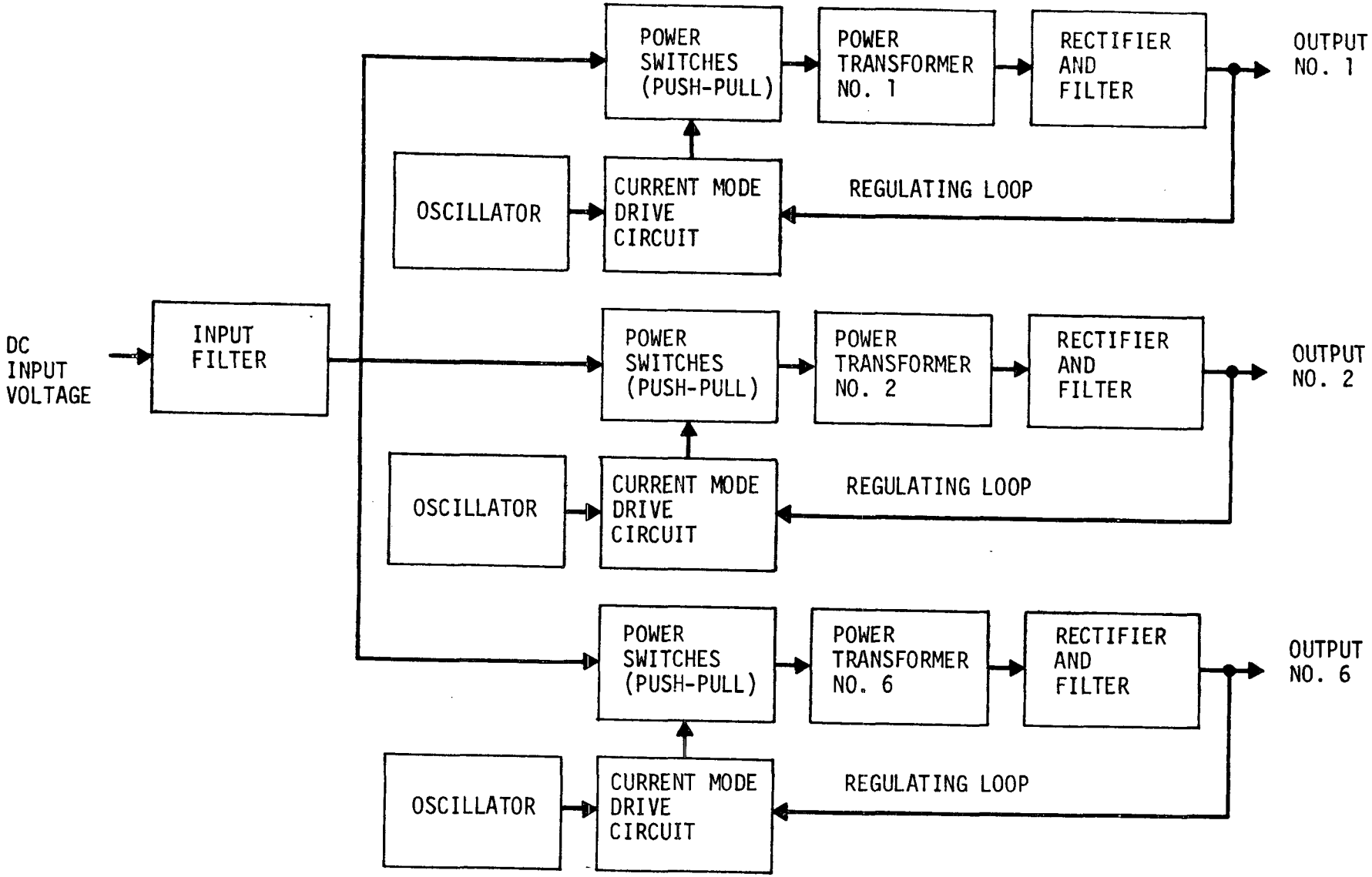

FIGURE 4-11. ARRANGEMENT 4

uses the dc-to-ac inverter and rectifier combination, but instead of using the dc-to-ac inverter as a simple power converter, the "ON" and "OFF" times of each switch are controlled in such a manner as to obtain output voltage regulation.

Two deficiencies are associated with this arrangement. First, each regulated output from the power supply requires a separate inverter and drive circuit. While this was not a basic deficiency of the arrangement, it results in a more complex overall design of the power supply. Second, providing stable, closed-loop control of a regulator around the power transformer becomes very difficult when a conventional control concept is employed. Basically, this condition results from the transformer introducing a second-order response into the control transfer function, causing unstable closed-loop operation.

A detailed analytical investigation of the control loop disclosed that the second-order break could be eliminated if a different mode of control was utilized. Since any impedance, including a transformer, does not affect the output current from a true current source, operation of the regulating inverter as a voltage programmable current source would eliminate the stability problem. This mode of operation has an additional advantage in that it provides inherent short-circuit protection since a current source can only supply a fixed, maximum current level to a short circuit.

Calculations of the efficiencies of arrangement 3 and arrangement 4 were performed to allow an estimate and comparison of their efficiencies. The improvement in the efficiency of arrangement 4 can be seen by comparing the two for when each is supplying power to two different load requirements. In the first requirement, the

circuit is supplying 150 watts at 28 volts (I_{load} = 5 amperes, approximately) and in the second the circuit is supplying 150 watts at 5 volts (I_{load} = 30 amperes). The calculated efficiency data for these two cases are shown in Table 4-1.

TABLE 4-1. COMPARISON OF POWER SUPPLY EFFICIENCIES FOR ARRANGEMENTS THREE AND FOUR

LOAD (150 W)	EFFICIENCY (%)	
	ARRANGEMENT 3	ARRANGEMENT 4
28 V at 5.4 A	91.6	94.0
5 V at 30 A	78.7	86.0

The improved efficiency of arrangement 4 is more impressive if the power losses in watts are compared. At a 5-volt, 150-watt output level, a regulator which is 86 percent efficient dissipates approximately 25 watts. The power dissipation of a regulator supplying the same load, but at 78.7 percent efficiency, is 40 watts, or 15 watts greater than the first case.

Arrangement 4 is more complex than arrangement 3 if only the total parts count of the two are considered. However, it must be noted that most of the additional parts are small, low-stress-level components, most of which can be incorporated into hybrid integrated circuits that may be used in the design. For this reason, the added complexity will not significantly degrade the overall reliability of the power supply.

The efficiency improvement of arrangement 4, which utilizes the dc-to-ac inverter as a pulse-width-modulated regulating element, provides a significant power savings — almost two-to-one at 5.0 volts — over arrangement 3. This power savings, coupled with the fact that complexity, size, weight, and reliability are not compromised, make it the choice for the optimum power supply arrangement. The configuration selected was a push-pull inverter with "current drive", since this type of inverter performs better than any other configuration with respect to all the tradeoff parameters.

4.3.3 Detailed Circuit Design

The evaluations and analyses discussed above led to the selection of an optimum basic arrangement for the standard power supply design. The result of the efforts was a simplified, functional block diagram for the power supply. The next step in developing a complete design for the power supply was to add the necessary supporting functions to the basic design to provide all of the operational capabilities required from the supply. Examples of these supporting functions are an oscillator, control circuits, failure indication, etc. When these were added, the design assumed the configuration shown in Figure 4-12.

After the block diagram configuration had been established, the major design effort associated with Phase II was begun. The effort was divided into four major areas which are relatively independent of each other. This approach allowed independent analysis and a detailed design effort for each area, the results of which could then be combined to establish an overall detailed design. The four major areas were:

- Power Circuit Magnetics and Inverter Design
- Input and Output Filter Design
- Energy Storage
- Control Circuit Analysis and Design.

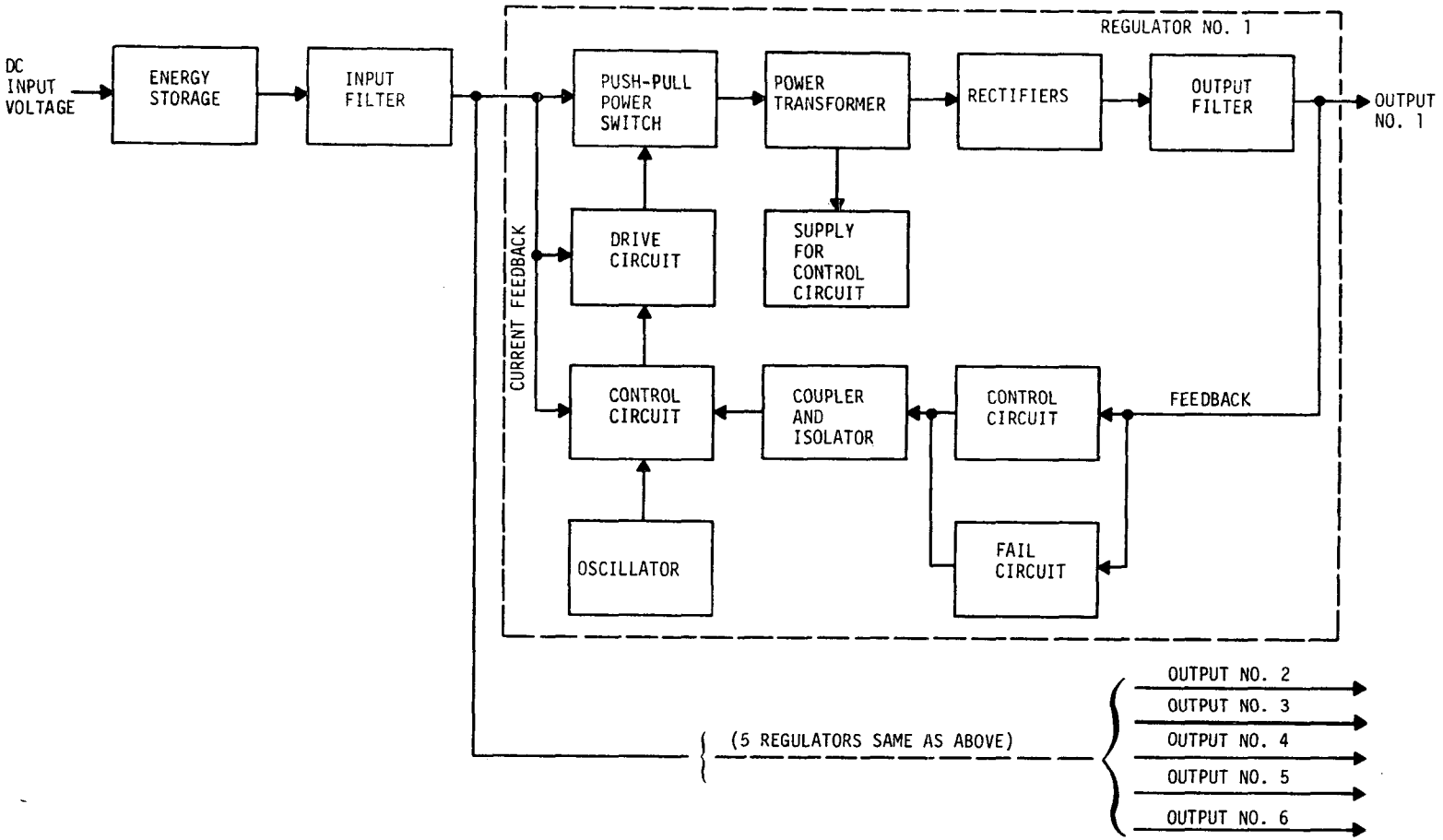

FIGURE 4-12. COMPREHENSIVE BLOCK DIAGRAM OF SELECTED POWER SUPPLY DESIGN

The guidelines used in this effort were established by the specification generated as the result of Phase I (see Appendix A) and the guidelines established for the tradeoff studies (Section 4.2). In addition, good design practices and the fact that the designs must be compatible with hybrid integrated circuit techniques were considered.

4.3.3.1 Inverter Power Circuits and Magnetics

4.3.3.1.1 Power Transformer Analysis - The overall performance of the inverter, particularly with respect to efficiency, is greatly influenced by the design of the power transformer. Since this one component in the circuit plays such a significant role in the operation of the power supply, a very thorough tradeoff analysis was performed to establish an optimum design for the transformer. The intent of this analysis was to derive a general relationship between the transformer losses and the following factors:

- Size of the transformer core
- Magnetic material from which the core is constructed
- Frequency of operation of the inverter
- Number of turns of wire used on the primary winding of the transformer.

The complete analysis is given in Appendix C.4 of this report. Briefly, the results of the analysis show the following:

- With respect to losses, a ferrite material is far superior to the best tape wound cores for cores of the same size
- Increasing the operating frequency of the inverter reduces the total losses of any of the transformer designs evaluated. (Note that this is total losses.) This can be seen from curves C.4-2, C.4-3, and C.4-4 in the appendix.

The information developed in the tradeoff analysis was used to design a very low loss transformer for the power supply. The design does not provide the ultimate in low losses, however, because certain practical considerations affected the design. Most significant of these is that the turns per volt of the primary winding must be chosen such that a reasonable number of turns results on the secondary. For example, it would be undesirable to use a winding ratio which resulted in one and one-half turns of wire on a low-voltage secondary of the transformer, as might be the case for a 5-volt output. Also, power losses caused by high speed switching of the active devices are directly proportional to operating frequency. These can become excessive if the switching frequency is made too high in an effort to minimize transformer losses. The requirement for minimizing the size and weight of the overall supply prevented the use of extremely large cores.

4.3.3.1.2 Power Switching Devices - The power switching transistors and the power rectifier diodes, as noted in the preceding section, are of particular interest in the design of the power supply. Since they have a finite switching time with the associated losses, these devices are the major factors determining operating frequency in a power supply design. It is obvious that the transistors and diodes selected must have short switching times as compared with the period of the operating frequency.

Storage time in the transistor, although not generally as important as rise and fall switching times, must also be considered, since this parameter limits the minimum time that the transistor can be conducting and, therefore, the minimum duty cycle of operation.

Other characteristics of the power semiconductors affect the operation of the power supply. A list of the important switching

transistor and power diode parameters which are of particular interest in the standard power supply is given in Table 4-2. A description of how these parameters affect losses with increasing frequency is presented in detail in Appendix C.5.

TABLE 4-2. PERTINENT SEMICONDUCTOR PERFORMANCE PARAMETERS

TRANSISTORS	DIODES
• Rise and Fall Switching Time • Storage Time • Collector Saturation Voltage • Collector Leakage Current • Saturated Forward-Current Transfer Ratio	• Forward Voltage Drop • Reverse Recovery Time • Reverse Voltage Leakage Current

Semiconductor losses increase with increasing frequency. The transistor frequency dependent losses are due primarily to their finite rise and fall switching times, whereas the diode frequency dependent losses are due to their reverse recovery times.

4.3.3.1.3 Current Mode Drive Circuitry - It has been noted that "current-mode drive" inverters have advantages in lower power dissipation over inverters which employ voltage drive. When properly designed, the efficiency of the current-mode drive inverter will be nearly constant over a wide range of loads because its base current is proportional to load current. The use of a constant forced gain also enhances the overload capability and operating characteristics of this type of inverter.

Transistor switching parameters as well as saturation voltage (the two most important efficiency-determining parameters), are

greatly affected by the base drive characteristics. Care must be exercised with regard to the design of the base drive circuitry in order to optimize these parameters.

The collector-to-emitter saturation voltage of a transistor is determined to a great extent by the amount of base drive at a given collector current. However, losses in the base circuit are directly proportional to the amount of base drive. It is, therefore, equally important to supply enough base current to maintain transistor saturation as it is not to excessively overdrive the transistor, thereby minimizing base losses.

Transistor rise and fall times and storage time are affected by the magnitude of the drive current. The rise time is directly proportional to the forward base current, and fall time is directly proportional to the amount of reverse "sweep out" base current. The storage time is a function of both the forward and reverse base current. These static and dynamic transistor charactertistics dictate the performance specification of the base drive circuitry. Since transistor specifications vary within device types, optimization must be performed on maximum, or worst-case, device specifications in order that the design will perform as required under these worst case conditions. A complete analysis of these transistor parameters, as they related to base drive, is given in Appendix C.6.

The requirements established by this analysis led to the development of a base drive circuit shown in Figure 4-13 for the power supply.

This circuit has several desirable performance characteristics, in addition to being extremely efficient and uncomplicated.

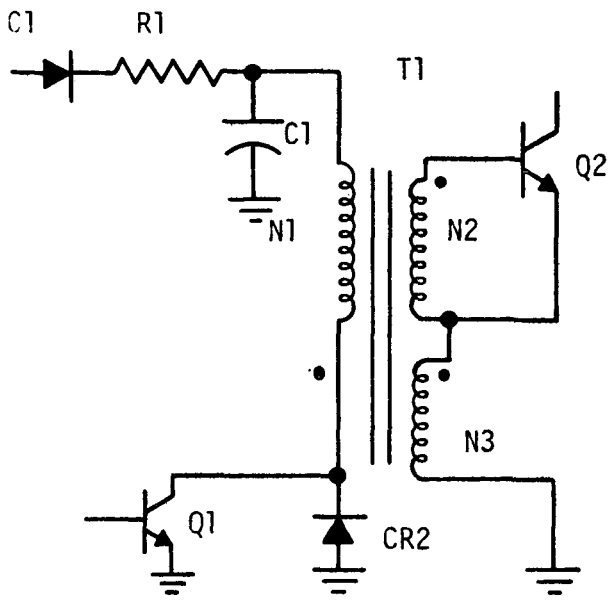

FIGURE 4-13. CURRENT-MODE DRIVE CONFIGURATION

In this circuit the base drive current is proportional to the collector current as shown by the following equation:

$$I_B = \left(\frac{N_3}{N_2}\right)\left(I_C\right) + I_M$$

where

I_B - base current

N_2 - number of turns of base winding

N_3 - number of turns of emitter winding

I_C - collector current

I_M - magnetizing current in transformer.

This allows for selection of the forced base drive level by varying the turns ratio of N_2 to N_3.

Since the forward base current has a component of current equal to the magnetizing current, the current is large at turn-on, minimizing rise time. Also, since the magnetizing current acts as an instantaneous current source, the voltage across the N_2 winding (V_{BE}) will rise to the value necessary to cause that current (I_M) to flow, minimizing delay time.

When transistor Q1 is turned on to drive the power transistor Q2 off, the reverse base current is limited only by the impedance represented by capacitor C1, transistor Q1, and the dc winding resistance of the transformer. This produces a high reverse current drive, minimizing fall and storage switching times.

Care was maintained with regard to transformer design to minimize leakage inductance since this degrades switching performance of the drive circuitry.

4.3.3.2 Design for Input and Output Filters - The primary function of the input and output filters is to suppress to acceptable limits the alternating line current generated by the switching action of the power supply. The limits for the standard power supply were selected to be those specified by Military Standard MIL-STD-461A, Amendment No. 3, for the input filter, and by the output ripple limit specified in the power supply specifications for the output filters (see Appendix A).

4.3.3.2.1 Input Filter - The first aspect considered was the configuration of the input filter, e.g., a single-section or multi-section LC-type filter. Considerable study effort has been performed on the design aspects of single-section and two-section LC-type input filters (see Ref. 3). The results of the analyses showed that:

- Two-section filters can offer significant size and weight savings when attenuation required is less than -20 decibels at the operating frequency (approximately 20 to 50 percent weight savings).

- Single-section filters are more efficient than two-section filters for a given requirement (approximately 50 percent power savings in the filter).

- Two-section filters have higher attenuation versus frequency characteristics (two to one)

- Two-section filters can be designed to be relatively immune to input transients and have the advantage of being able to reduce the magnitude of the start-up inrush current.

Generally, conflicting design implications exist since a compromise must be made to obtain the best overall configuration.

To meet the requirements of MIL-STD-461A, the power supply requires input filter attenuations greater than -20 decibels at the operating frequency. Hence, a single-section filter was chosen as the optimum filter configuration for the power supply. This choice results in a considerable improvement in weight, size, and efficiency of the single-section filter when compared with the two-section filter. To offset the somewhat degraded performance of the single-section filter, the input filter package for the power supply will contain a small, tubular RFI filter in each line which will attenuate the very high-frequency ripple currents to acceptable levels. The inclusion of such an RFI filter will make the performance of the single-section input filter compatible with the performance of the two-section filter without compromising efficiency, size, or weight. An analysis of the design of the filter components is shown in Appendix C.7.

The results of the analysis indicated that the size and weight of the input filter, for a given set of requirements, are directly proportional to the efficiency of the filter. An important note is that since

choke design relies heavily on capacitor performance, impedance characteristics, capacitance voltage product per unit volume, and the capability to handle ripple current, selection of a tantalum-type capacitor was mandatory to optimize both efficiency and filter size and weight.

4.3.3.2.2 Output Filter - The design criteria for the output filter, with regard to efficiency, weight, size, and performance, are identical to the criteria for the input filter. However, the capacitor requirements depend on both the inductor design and the closed-loop stability of the power supply. An analysis of the output filter design is presented in Appendix C.8. To complete the design, an appropriate value of capacitance must be selected to meet the regulator loop stability criterion. (This criterion is presented in Appendix C.10.) Once this has been selected, the inductor design is straightforward, as shown in Appendix C.8.

4.3.3.3 Design for Energy Storage Elements - Some loads which the power supply will service, such as computer memories, require non-interrupted power. However, power-source switching and input line transients result in short periods during which the input source power will drop out or fall below the minimum operating requirements of the power supply. To accommodate these loads, some means of energy storage must be provided in the power supply design. Therefore, the following methods of providing energy storage were considered:

- Capacitor
- Energy storage device (ESD)
- NICAD battery.

Each of these devices was analyzed for possible use in the proposed power supply. A summary of this analysis is shown in Appendix C.9.

Energy storage devices (ESDs) offer very high capacitance-to-unit volume ratios. However, the use of these devices in the power supply is impractical because of their high series resistance and extremely low voltage ratings; to offset these parameters, the devices must be excessively large. However, with further development, these units may be useful for this purpose in the future.

NICAD batteries are smaller in size than capacitors for an equivalent storage capability. However, when the cost and added complexity of a charger is considered, the total cost and volume required can become higher than a capacitor.

The results of the analysis show that a capacitor utilized as a storage device at the input of the power supply is preferred. However, if drop-out times are much greater than approximately 10 milliseconds, the cost and volume tradeoffs begin to favor NICAD batteries. For the standard power supply the use of tantalum capacitors is recommended as the energy storage device.

4.3.3.4 Analysis and Design of Power Supply Control Circuits - An analysis of the selected concept for the control circuit was performed to predict the performance of the power supply and the parameters that affect performance. These criteria, although significant, are general. Therefore, guidelines were required that would govern the actual circuit design. These guidelines are:

- Utilize state-of-the art components only when these components afford performance and size improvements at a reasonable cost.
- Utilize integrated circuits whenever possible to minimize cost, complexity, and size and to improve reliability.
- Utilize circuits and devices that offer low operating power drain to maximize efficiency and minimize component stress.

- Utilize circuit configurations and designs that are compatible with the present hybrid technology.

- Ensure that the circuit designs are compatible with good design practices to ensure a high degree of performance and reliability.

Utilizing the results of the analysis and the generated guidelines, a design was implemented that would ensure stability and performance compatible with the proposed power supply specifications. The detailed analysis of the control loop is shown in Section 4.5. The analysis shows that the circuit will be stable for all values of load current, input voltage, and load impedance. As noted earlier, the use of a current source type drive for the circuit negates the effects of the two poles introduced by the transformer.

4.4 ELECTRICAL DESIGN DESCRIPTION

The work performed on developing and analyzing an overall configuration for the power supply formed the basis for generating a detailed circuit design for the unit. Many of the design details including component values were derived from the analyses which were performed on the major functional elements of the supply. These analyses are documented in Appendix C. The detailed description of the selected design for the power supply can best be presented by describing its individual functional elements and their relationship to the operation of the supply. Figure 4-14 shows the complete schematic diagram of the supply and the following paragraphs present the description of how each element of the supply operates. The basic power supply circuit is a push-pull switching regulator. The operation of the circuit is as follows. The output load current is monitored at the primary winding of the power transformer and is

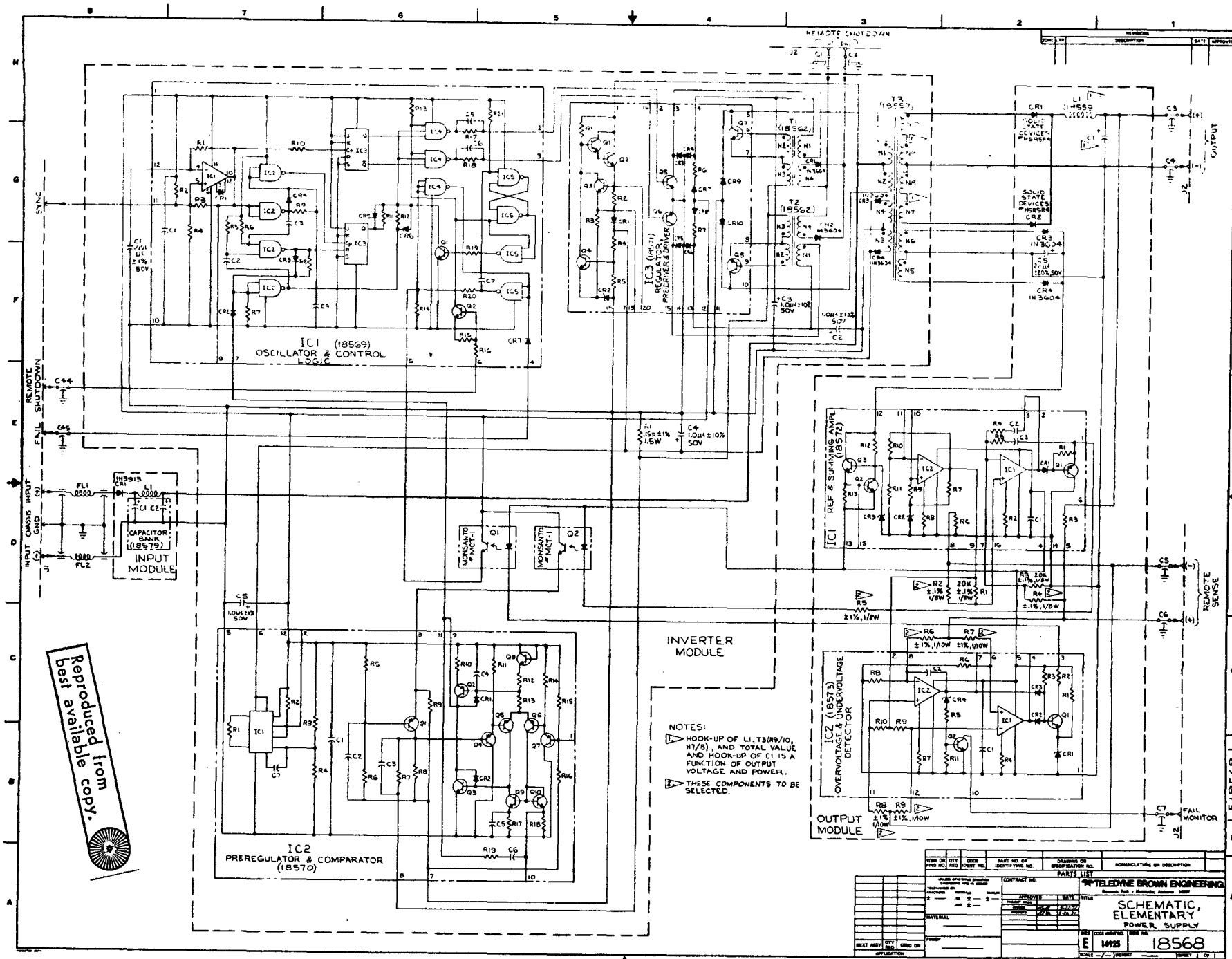

FIGURE 4-14. OVERALL SCHEMATIC DIAGRAM

compared, at the comparator, with an error feedback voltage. This error voltage, which is proportional to the difference between the output voltage and a reference voltage generated by the reference supply, is supplied to the comparator through an optical coupler from the summing amplifier. The optical coupler is used to maintain isolation between the primary and secondary grounds. When the load current, which is proportional to a voltage at the comparator, exceeds this error voltage, a pulse is generated at the output of the comparator and supplied to the control logic. This pulse causes the control logic to inhibit the power switch drive for the rest of the cycle. The control logic is then reset by the next oscillator clock pulse and the cycle repeats, providing pulse-width modulation. In essence, the control loop forces the load current to be that value necessary to produce an output voltage equal to the reference voltage.

A more detailed description of each element in the supply is given below. The pin numbers shown in the discussions are those which are assigned to the hybrid integrated circuits used in the design. These are described in detail in Section 5.

4.4.1 Oscillator

The oscillator circuit, shown in Figure 4-14 as part of the oscillator and control logic section, is configured around an operational amplifier (IC1). Resistors R1 through R4 and external capacitor C1 determine the oscillator frequency. The basic timing network consists of resistor R1 and capacitor C1 with resistor R3 providing the necessary positive feedback to ensure oscillation of the circuit.

The operation of the oscillator is as follows. The operational amplifier (IC1) is operated as a switch with its output being saturated

either in the high (positive) or in the low (ground) state. Resistors R2 and R4 provide a positive bias at the non-inverting input such that when the operational amplifier changes state it causes a corresponding change, determined by the values of resistor R3 and bias resistors R2 and R4, in this bias voltage. When the operational amplifier is saturated in the high state, the voltage at the non-inverting input equals the bias voltage (determined by R2 and R4) plus the feedback voltage. Also, since the output of the operational amplifier is high, the capacitor C1 begins to charge through resistor R1. When the voltage across the capacitor reaches a value approximately equal to the bias voltage plus the feedback voltage, the operational amplifier switches to saturation in the low state, and the voltage at the non-inverting input drops to a value equal to the bias voltage minus the feedback voltage. When this occurs, capacitor C1 begins to discharge through R1 until its voltage reaches a value equal to the bias voltage minus the feedback voltage, at which time the operational amplifier switches to saturation in the high state, and the cycle of the oscillation repeats.

Although the oscillator circuit is not complex, it offers good stability, determined primarily by the characteristics of the resistors and the capacitor used. Also, it exhibits low power consumption and can be synchronized with any similar oscillator or group of oscillators by paralleling all the oscillator non-inverting input terminals.

4.4.2 Control Logic

The control logic circuitry, shown in Figure 4-14 as part of the oscillator and control logic section, consists of two flip-flops [IC3 (a) and (b)] and several associated components. The first flip-flop [IC3 (a)], which is driven by the oscillator, provides the complementary drive necessary for the push-pull inverter. The second flip-flop is used

as a set and reset memory. This memory flip-flop [IC3 (b)] is gated with, and has the capability of controlling the output drive signal by inhibiting the two output drive gates [IC4 (a) and (b)].

When a positive reset pulse is received at Pin 7, the control flip-flop IC3 (b) inhibits the drive signal. Gates IC2 (a) and (b), resistor R5, and capacitor C2 form a monostable multivibrator which is used to ensure that the pulse width of the reset pulse into IC3 (b) is long enough to allow the control flip-flop to reset upon command. When the control flip-flop has been reset it will remain in the reset mode until it is set by the oscillator clock pulse.

Gates IC2 (a) and (b) perform two functions. The first function is to provide a delay, determined by resistor R9 and capacitor C4, in toggling the drive flip-flop IC3 (a). This delay, which is designed to be longer than the storage time for the power switching transistor, ensures that both power switching transistors cannot be conducting simultaneously. The second function of IC2 (a) and (b) is to provide a reset pulse in the control flip-flop at the end of the conducting period of each of the power switching transistors. This reset pulse is coupled through capacitor C3 to the monstable multivibrator formed by IC2 (c) and (d). This pulse assures that the drive signal will be inhibited at the end of each half cycle of drive and, in turn, that the conduction times of the power switching transistor will not overlap when no external reset pulse is present. To minimize time delays associated with the reset action of the control flip-flop [IC3 (b)], the inhibit command is fed around this flip-flop through IC2 (d) and resistor R12 to the output drive gates [IC4 (a) and (b)].

The additional circuits consisting of integrated circuits IC4 (c) and IC5 and transistors Q1 and Q2 (shown in Figure 4-14), provide remote shut-down and failure protection. For example, a signal representing the condition of the output regulated voltage (a relatively

low dc voltage represents an over-voltage or under-voltage condition), is entered at Pin 5. A low (ground) voltage level at this input (Pin 5) is coupled through IC4 (c) and outputed at Pin 4 as a high (positive) voltage, indicating a failure condition. If the regulated output terminal had been normal (if the voltage at Pin 5 had been high) and a failure condition appeared, the transition of the voltage at Pin 4 from a low (normal) to a high (fail) state would be coupled through C7 into the latch circuit formed by IC5 (a) and (b). This signal would set the latch and inhibit the drive signal by causing transistor Q1 to conduct. The drive signal would remain inhibited until the latch was reset by the receipt of a remote shut-down command at Pin 6. This command, which is implemented by a high (a positive voltage) at Pin 6, is coupled to the gates formed by IC4 (a) and (b) and functions as a remote shut-down feature. It also resets the fail circuitry.

The control logic was designed to utilize complementary metal oxide semiconductor (C-MOS) integrated circuits which provide high noise immunity while consuming very little power.

4.4.3 Pre-Regulator and Comparator

The pre-regulator and comparator circuitry is shown in Figure 4-14. The pre-regulator section, which serves as the power supply for the control circuit on the primary side, derives its power from the main power transformer (T3), from windings N3 and N4. The circuit is composed of an integrated circuit regulator (IC1). This regulator provides the voltage regulation required by the comparator circuit, and affords minimal size and power consumption.

The comparator circuit, consisting of transistors Q2 through Q10, is basically a high-speed differential amplifier. The comparator has been designed to measure relatively low signal levels, on the order

of a few hundred millivolts full scale with respect to ground, and to utilize a single operating voltage, thus simplifying the housekeeping circuits. Because a commercial integrated circuit comparator that would perform satisfactorily was not available, it was necessary to design a discrete differential comparator.

The operation of the circuit is as follows. When the voltage at the base of transistor Q4 is lower than that voltage present at the base of Q7 (determined by the value of resistors R15 and R16 and the supply voltage), transistor Q4 conducts, causing transistor Q5 to conduct. When transistor Q5 conducts, the voltage at the emitter of Q5 becomes lower than that necessary to cause transistors Q6 and Q7 to conduct; therefore, transistors Q9 and Q10 also are non-conducting. The current flowing in the collector of transistor Q5 then flows into the base of transistor Q3, causing it to conduct. This drives the output signal of the comparator (Pin 9) low.

When the voltage at the base of transistor Q4 exceeds that voltage present at the base of Q7, transistors Q4 and Q5 turn off and transistors Q6 and Q7 conduct. The collector current flowing from transistor Q6 turns transistors Q9 and Q10 on, clamping the base of transistor Q3 below its conduction voltage. With transistor Q3 off, the output signal of the comparator is driven high (positive) through the current source formed by transistors Q2 and Q8 and resistors R10 and R12. Diodes CR1 and CR2 clamp their respective transistor base-to-collector voltage such that they cannot saturate, eliminating their saturated time delays. The switching time of the comparator is essentially that of the output drive transistor Q3. Positive feedback, provided by the network consisting of resistor R19 and capacitor C6, ensures that the output of the comparator will be free from noise.

The power supply current feedback signal, which is a voltage measured across resistor R1 (a 0.15 ohm, 1.5 watt resistor), is proportional to the load current. This feedback signal is summed together with the error voltage from the output circuit through Pins 8 and 3, respectively. Transistor Q1 provides a low impedance load for the optical coupler, and also provides isolation between the optical coupler and the current feedback signal.

A tradeoff must be made in the design of the comparator between power consumption and speed. The circuit was designed to provide high speed performance; this required a sacrifice, to a minor extent, in power consumption .

4.4.4 Start-Up Regulator

The start-up regulator, shown in Figure 4-14 as part of the regulator, pre-driver, and driver section (IC3), is designed around transistors Q1 through Q4. The regulator is a series pass type, with transistors Q1 and Q2 forming the darlington series pass transistors and transistors Q4, zener diode CR2, and resistors R4 and R5 forming the feedback and control circuitry.

This internal regulator provides the voltage required to run the control circuitry when power is not supplied by the power transformer (T3), which would be the case when the power supply was shut down and/or during a fault condition. The output regulated voltage provided by the regulator is designed to be lower than the voltage provided by the power transformer such that during normal operation, when power is supplied by the main power transformer, this regulator will shut down.

The basic operation of the circuit is as follows. When power is applied to the input of the supply, the input line voltage is applied to Pin 1 of this section and Pin 18 referenced to ground. The voltage at the base of transistor Q1 with respect to ground is adjusted by transistor Q4 such that the voltage impressed at the base of Q4 to ground equals the voltage of the zener diode plus the base-to-emitter voltage of Q4. The voltage at the base terminal of transistor Q4 is fixed and therefore the voltage at the output terminal of the regulator (Pin 17) is fixed since resistors R4 and R5 form a simple voltage divider network. Resistor R3 provides the current to the zener diode required to establish a reference voltage, and resistor R1 provides the necessary base drive to the darlington series pass transistors.

Current limiting is provided by the circuit consisting of transistor Q3 and resistor R2. When the load current is such that the current produces a voltage drop across resistor R2 equal to the base-to-emitter conduction voltage of transistor Q3, Q3 conducts, shunting the base drive from the darlington series pass transistors Q1 and Q2. This action limits the maximum current available, providing current-limiting and short-circuit protection.

4.4.5 Pre-Driver and Driver

The pre-driver and driver circuitry, shown in Figure 4-14 as part of the regulator, pre-driver and driver section, is designed around transistors Q5 through Q8. Since this element contains two identical and independent circuits, the explanation of only one of these circuits will be given, simplifying the discussion. One of these circuits is redrawn in Figure 4-15 and, for the purpose of this discussion, is shown with the magnetizing inductance represented by the base drive transformer (T1) modeled as L_m.

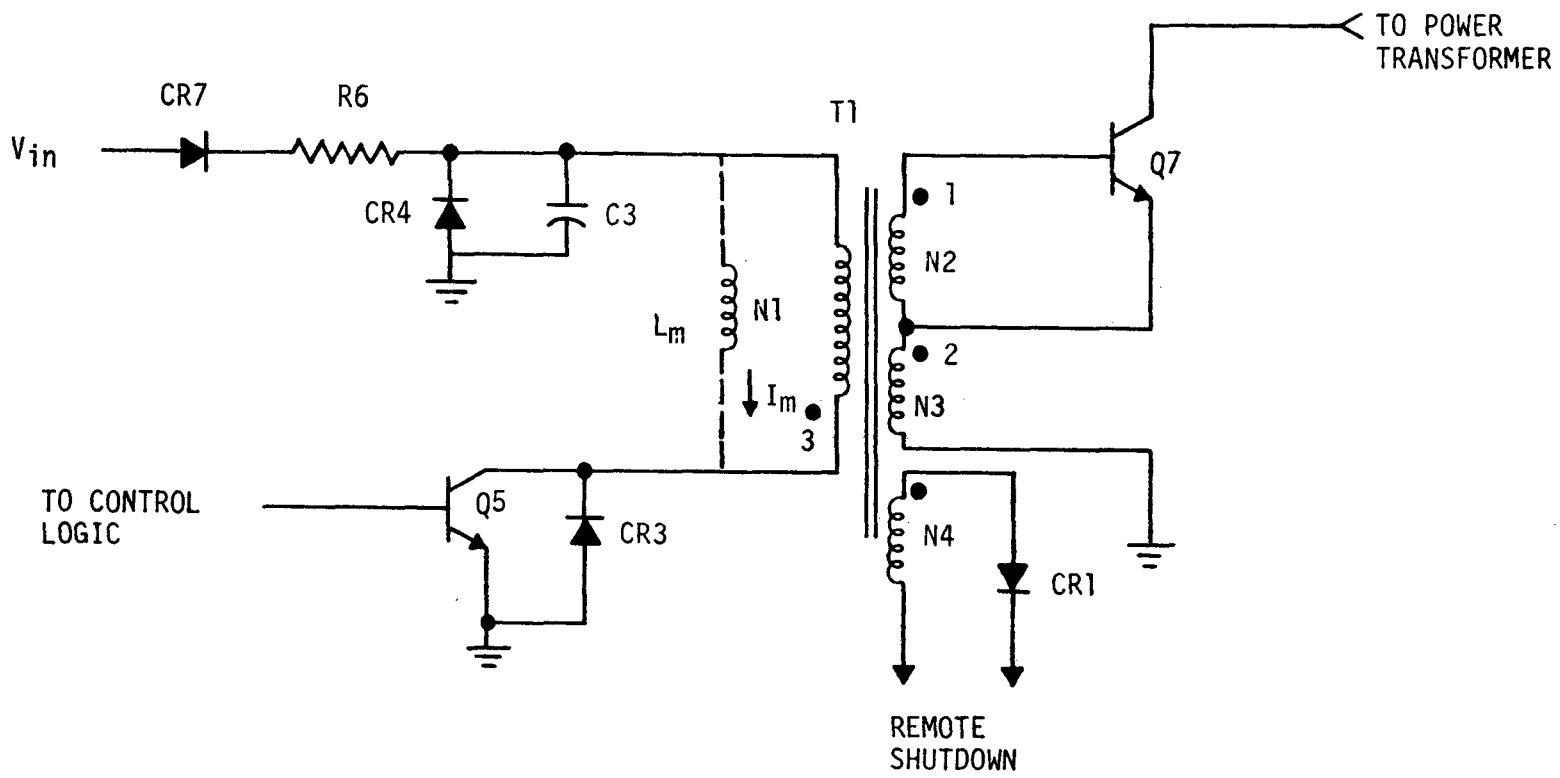

FIGURE 4-15. PREDRIVER AND DRIVER CIRCUIT DIAGRAM

The circuit operation is described as follows. Initially, with transistor Q5 conducting, the secondary winding is essentially open circuited, since the base-to-emitter terminals of transistor Q7 are reverse biased, and current flows in the primary winding (N1). This current, assuming zero initial conditions, increases at a rate determined by the inductance of primary winding (N1) and circuit resistance; i.e.,

$$i_m(t) \simeq \frac{V_{in}}{R6} \left[(1 - \exp(-R6/L_m\, t)\right]$$

where

$i_m(t)$ - the magnetizing current flowing in the primary winding (N1), when Q5 is conducting

V_{in} - input voltage to drive circuit

t - time.

When Q5 is turned off, which open-circuits the primary winding, the energy which was stored in the primary magnetizing inductance (L_m) discharges into the secondary winding. This may be represented as a current flowing out of the magnetizing inductance L_m into the primary winding N1 (into point 3 in Figure 4-15), which causes a current from the secondary winding (N2) to flow into the base of Q7. This current decays at a rate proportional to the base-to-emitter voltage of Q7 and can be expressed as:

$$i(t) \simeq \left[I_o - \frac{V_{BE(Q7)} \frac{N_1}{N_2}}{L_m} \times t \right] \frac{N_1}{N_2}$$

where

I_o - value of the magnetizing current immediately before transistor Q5 is turned off [measured at the primary winding (N1)]

$V_{BE(Q7)}$ - base-to-emitter voltage of transistor Q7

L_m - magnetizing inductance measured at the primary winding (N1)

t - time

N_1 / N_2 - ratio of the primary to secondary winding

i(t) - the base current flowing into transistor Q7, due to the energy stored in the magnetizing inductance.

The base current into transistor Q7 turns this transistor on, causing collector current to flow through winding N3 of the base drive transformer (T1). This current, flowing in winding N3, causes additional current to flow in the base winding which is proportional to the turns ratio of windings N2 to N3 and the collector current, or

$$I_{b(Q7)} = \frac{N_3}{N_2} \left[IC_{(Q7)} \right]$$

where

$Ib_{(Q7)}$ - base current of transistor Q7, due to current flow in winding N_3

$IC_{(Q7)}$ - collector current of transistor Q7.

The total current flowing into the base circuit is then the sum of the current provided by the collector current flowing in winding N3 and the current provided by the energy stored in the magnetizing inductance (L_m). While transistor Q7 is conducting, the resultant current in the emitter winding of the base drive transformer (N3) causes the voltage

measured across the primary winding to be positive at point 3 (Figure 4-15) and capacitor C3 charges toward the input voltage (V_{in}) through resistor R6. When transistor Q5 is turned on, current flows through the primary winding [out of point 3 (Figure 4-15)], from capacitor C3 and resistor R6, drawing current out of the base of transistor Q7 and turning Q7 off. At the instant that transistor Q5 turns on, this current is large, limited only by the winding resistances, leakage inductances, and impedance of capacitor C3, and provides a large turn-off current at the base of Q7. During the time that transistor Q5 conducts the magnetizing current again increases, recharging the magnetizing inductance; thus, the cycle repeats.

Diode CR3 is included to protect the circuit for the case when the magnetizing current may reverse direction during operation. Such reverse direction would be caused by start-up transients or during long duty cycle operation at reduced frequencies. If the magnetizing current is flowing in the reverse direction (toward capacitor C3) when transistor Q5 is conducting, diode CR3 provides a path to ground such that this current will discharge into capacitor C3.

Diode CR4 is provided to prevent the inductor-capacitor network formed by the magnetizing inductance (L_m) and capacitor C3 from ringing, which would cause faulty triggering of the output power transistor Q7. Diode CR4 protects the network by preventing the capacitor voltage from going negative, due to magnetizing current; a negative voltage would result in a current flow in the direction to provide base drive for transistor Q7.

4.4.6 Reference Amplifier

The reference amplifier, shown in Figure 4-14 as part of the reference and summing amplifier section, is designed around operational amplifier IC2. The amplifier is operated in the non-inverting mode. The gain of the amplifier, determined by resistors R10 and R11 [Gain = (R10/R11 + 1)], amplifies the reference voltage established by zener diode CR2. The zener current is easily programmed by adjusting the value of resistor R7. In essence, the stable zener voltage stabilizes its own zener current. This scheme offers an extremely stable voltage reference. The output voltage (Pin 9) can be expressed as

$$V_o = V_z \left[\frac{R10}{R11} + 1 \right]$$

and the zener current may be written as

$$I_z = \frac{V_o - V_z}{R7} = \frac{V_z \times \frac{R10}{R11}}{R7} .$$

4.4.7 Summing Amplifier

The summing amplifier, shown in Figure 4-14 as another part of the reference and summing amplifier section, is designed around operational amplifier IC1 and transistor Q1. The operational amplifier is operated in the inverting mode with transistor Q1, which is configured as an emitter-follower, serving as an output drive stage. The zener diode CR1 functions as a level shifter coupling the output of the operational amplifier to the base of transistor Q1. The gain of this amplifier is determined by the ratio of the impedance of the feedback

network, consisting of resistors R4 and R5 and capacitors C2 and C3, to the resistance represented by external resistor R4. This amplifier compares the reference voltage derived from the reference amplifier and conditioned by an external resistor network consisting of R1 and R2 and the power supply output voltage, which is conditioned by an external resistor network consisting of R3 and R4. This amplifier provides the error feedback voltage, equal to the amplifier gain times the difference between the reference and the output voltage, which is coupled through the optical isolator to the comparator circuit, forming part of the power supply regulatory loop.

The additional circuitry in this section, consisting of transistors Q2 and Q3, comprises the output control circuitry regulator. The regulating element, consisting of transistor Q3 and zener diode CR3, forms a simple series regulator which derives its power from windings N6 and N5 of the main power transformer (T3). Transistor Q2 and resistor R13 provide a current-limiting feature which protects the regulating pass transistor Q3 from excessive dissipation caused by overloads.

4.4.8 Over-Voltage and Under-Voltage Detectors

The fault protection circuitry is contained in the over-voltage and under-voltage detector section shown in Figure 4-14.

The over-voltage circuitry is designed around an operational amplifier (IC2) in this hybrid. This amplifier compares the output voltage, entered at Pin 8 through the resistor network consisting of R8 and external resistor R6, with the reference voltage, entered at Pin 2 through the resistor network consisting of R10 and external resistor R8. When the input voltage exceeds a predetermined value, adjusted by external resistors R8 and R6, the output of the operational

amplifier is driven from saturation in the positive direction to saturation in the negative (ground) direction. When the amplifier is driven to ground it simultaneously drives transistor Q2 off, indicating a failure, and transistor Q1 off, initiating a shut-down command to be entered through the optical isolator (MCT1) into the control logic circuits.

The under-voltage detector, comprised of operational amplifier IC1, operates in a manner similiar to the over-voltage detector. When the input voltage (Pin 6) decreases below a predetermined value, adjusted by external resistors R7 and R9, the output of the operational amplifier is driven to ground which initiates a shut-down command to the inverter.

4.5 CALCULATED ELECTRICAL PERFORMANCE

The calculated electrical performance of the power supply meets or exceeds all of the initial specifications for the power supply, determined during Phase I of the study (outlined in Appendix A). The predicted performance of the power supply, based on an analysis of the supply under worst-case conditions, is presented in the following sections.

4.5.1 Control Loop Stability

An analysis of the control loop of the power supply shows that the system is stable and is optimally damped. The phase and magnitude plot of the open-loop transfer function is shown in Figure 4-16. From this curve the phase margin (ϕ_m) and the gain margin (G_m) can be obtained:

$$\phi_m \simeq 60 \text{ degrees}$$

$$G_m = +10 \text{ decibels.}$$

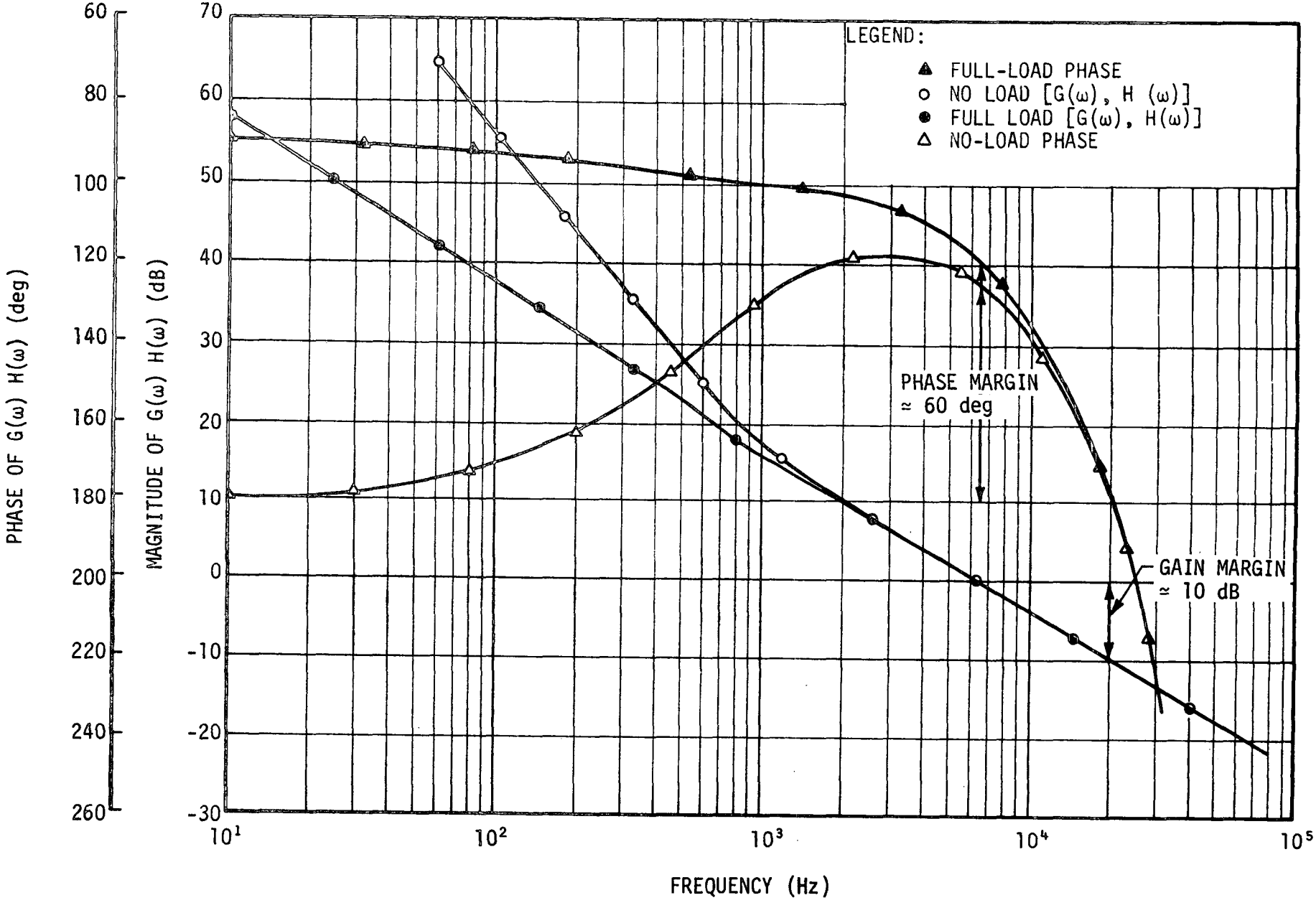

FIGURE 4-16. MAGNITUDE AND PHASE OF POWER SUPPLY OPEN LOOP TRANSFER FUNCTION

From these data the system damping ratio can be calculate as

$$\zeta \approx 0.01\ \phi_m = 0.60.$$

This shows that the system is optimally damped and unconditionally stable for any load.

The open-loop response is shown replotted on a Nichols diagram (Figure 4-17) to obtain the closed-loop transfer function shown in Figure 4-18. Although the closed-loop transfer function is not required for the performance analysis of the power supply, it provides conclusive evidence of the stability of the loop.

4.5.2 Input Characteristics

The input characteristics of the power supply are shown in Table 4-3.

TABLE 4-3. INPUT CHARACTERISTICS OF THE POWER SUPPLY

CHARACTERISTIC	VALUE		
	MINIMUM	NOMINAL	MAXIMUM
Input Voltage (Vdc)*	60	90 to 125	225
Input Ripple	Compatible with MIL-STD-461A, Amendment 3		
Efficiency (%)	86**		

*The power supply is capable of withstanding a continuous reversal in the polarity of the input voltage without damage. Recovery to normal operation is automatic when normal polarity is reestablished.

**This is the calculated minimum, worst-case efficiency at the nominal input voltage range for an output voltage equal to or greater than 5 volts, delivering 50 watts.

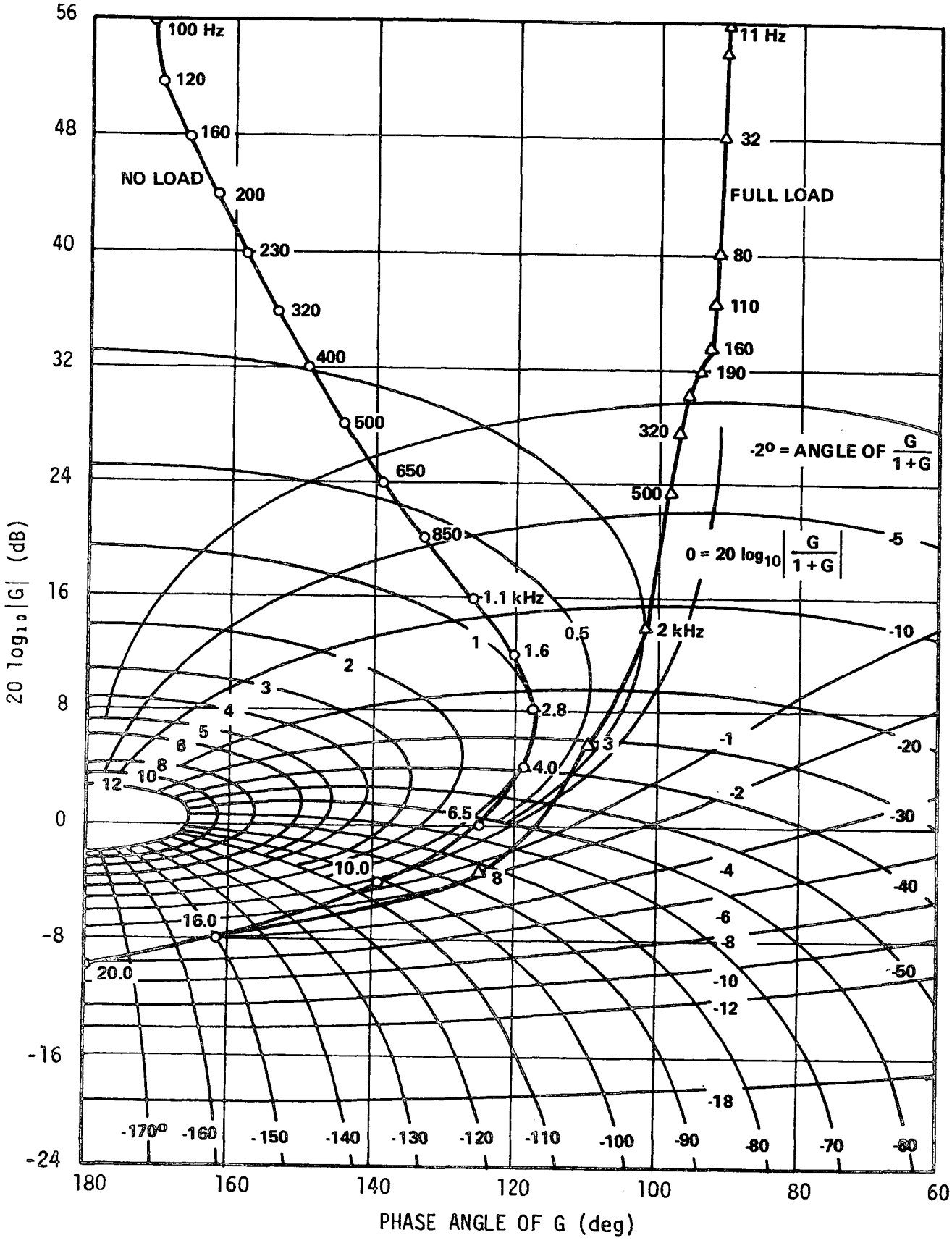

FIGURE 4-17. LOGARITHM MAGNITUDE-ANGLE DIAGRAM OF POWER SUPPLY TRANSFER FUNCTION

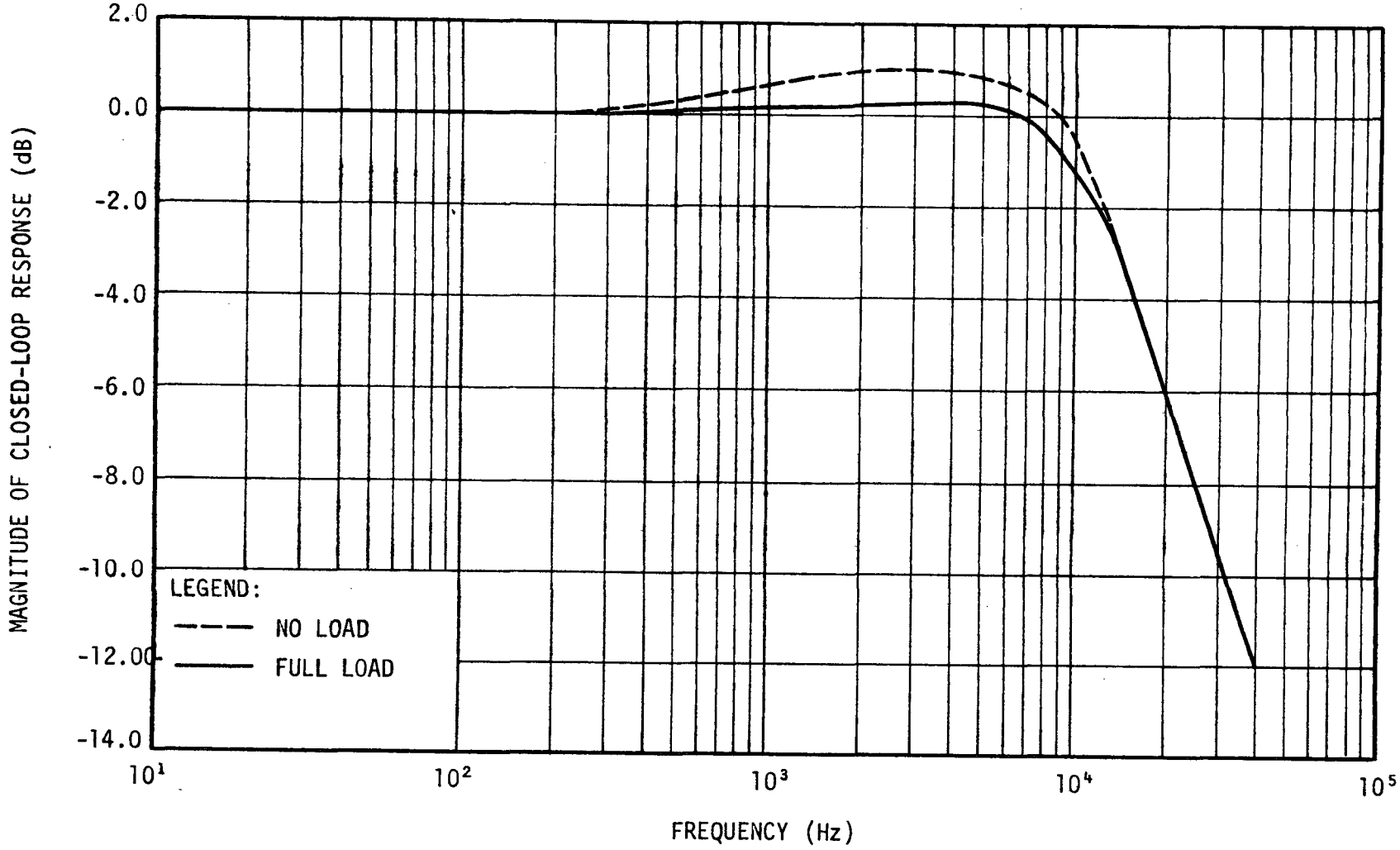

FIGURE 4-18. MAGNITUDE OF THE CLOSED-LOOP TRANSFER FUNCTION OF THE POWER SUPPLY

4.5.3 Output Characteristics

A summary of the output characteristics of the power supply is shown in Table 4-4.

TABLE 4-4. OUTPUT CHARACTERISTICS OF THE POWER SUPPLY

CHARACTERISTIC	VALUE
Output Voltage Range (V)	±5, ±10, ±15, ±30, ±45, ±90 (±20% adjustment capability on each nominal output voltage)
Load Transient Response* (No load to full load or full load to no load)	±29% of Rated Output Voltage for a Maximum Duration of 3 msec* (see Figure 4-19)
Line Regulation (Input voltage variation of 60 V to 225 V)	±0.002% of the Output Voltage
Load Regulation (No load to full load)	±0.02% of the Output Voltage
Temperature Coefficient (-20 to 85°C Ambient Temperature)	0.005%/°C of Output Voltage
Output Ripple Voltage (Peak to Peak)	0.4% of the Output Voltage
Output Impedance**	See Figure 4-20

*The no load to full load and full load to no load transient response is shown in Figure 4-19. Obtaining a load transient response of this control system is extremely difficult since the system is non-linear. However, a worst-case approximation to the load response can be obtained by considering the response of the output filter network to a unit step load change (no load to full load) and by considering the energy stored in the output choke (full load to no load).

**The output impedance of the power supply is shown in Figure 4-20. The curve is obtained by considering the output impedance of the filter network [$Z_O(\omega)$] and the open-loop gain at that particular frequency [$G(\omega)\ H(\omega)$] [Output Impedance = $Z_O(\omega)/1+G(\omega)\ H(\omega)$]. The curve shown in Figure 4-20 represents the dynamic load regulation of the power supply and is shown as a function of the maximum load resistance only. [Maximum Load Resistance = (Output Voltage)^2/Power Output at Full Load].

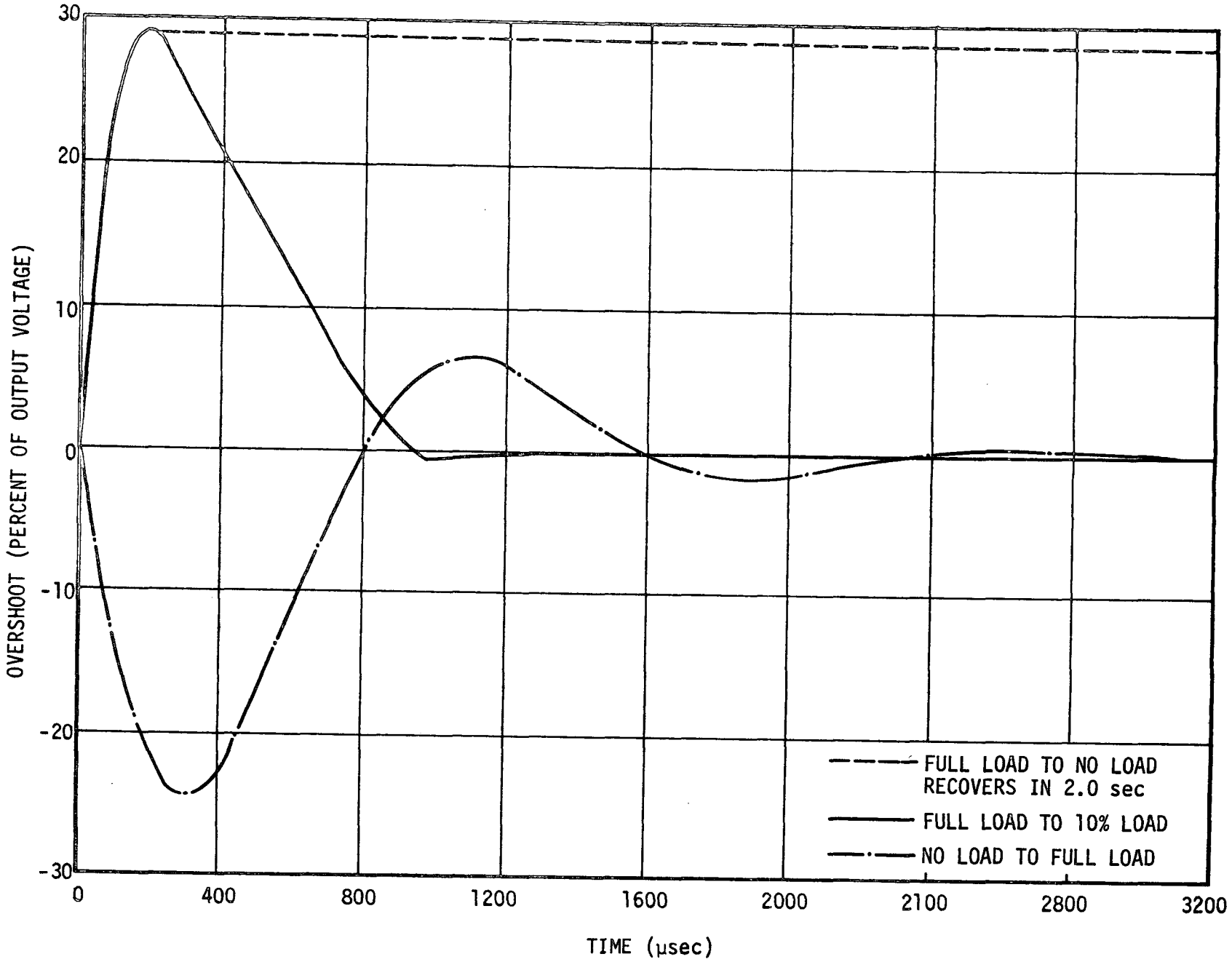

FIGURE 4-19. TRANSIENT LOAD RESPONSE OF POWER SUPPLY

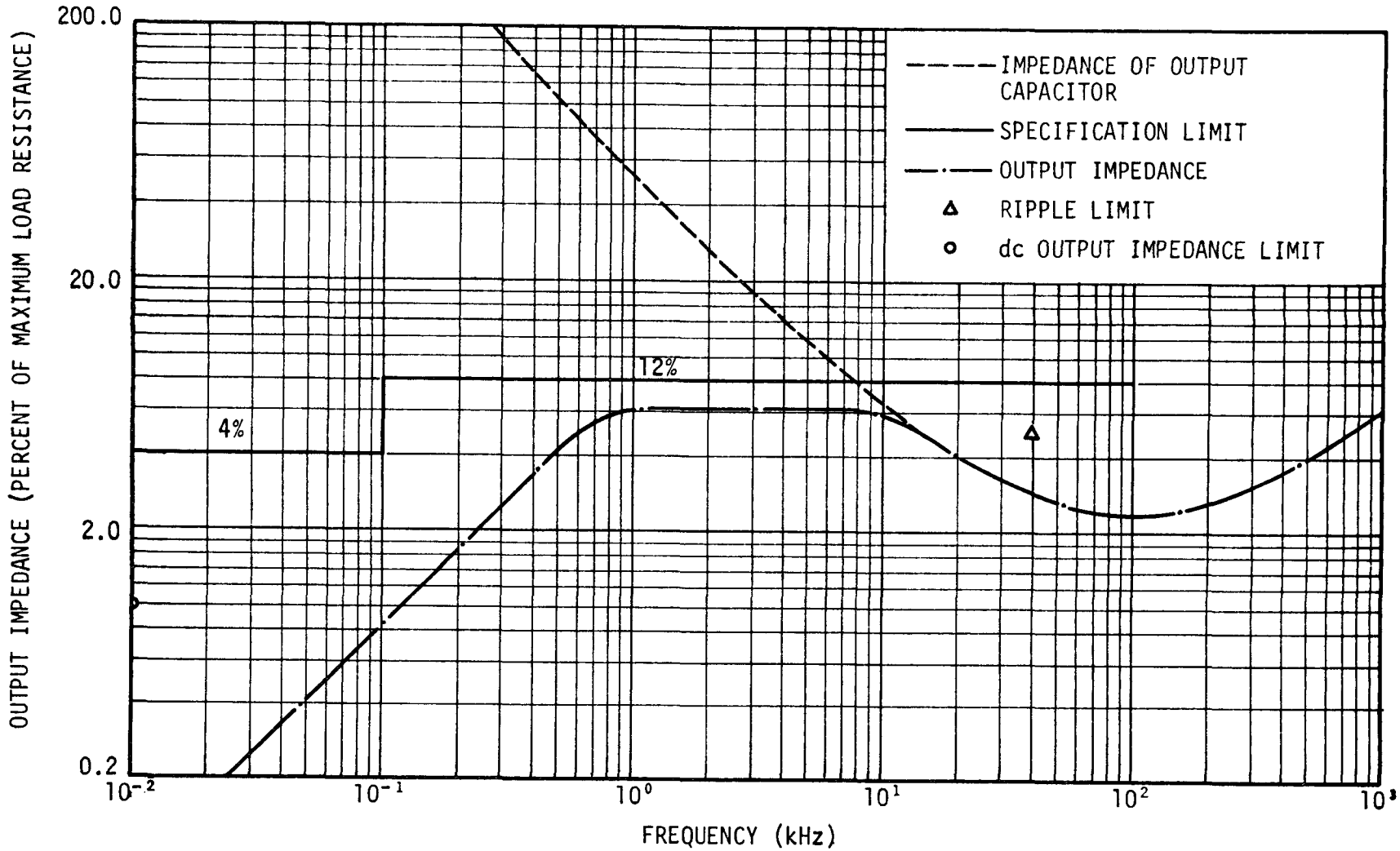

FIGURE 4-20. OUTPUT IMPEDANCE OF THE POWER SUPPLY AS A FUNCTION OF FREQUENCY

5. PHASE III ACTIVITIES AND ACCOMPLISHMENTS

The objective of Phase III of the study was to analyze the circuit design for the power supply and to select the portions which could be incorporated into the design as hybrid integrated circuits. Hybrid circuits offer greatly increased component packaging densities in an electronic design, with a resulting reduction in overall size and weight, and improved reliability of the circuit. For these reasons, it was considered essential that hybrids be incorporated into the power supply design to the greatest practicable extent. It should be noted that considerable thought was given to the use of hybrid circuits in the design during the Phase II efforts. For example, the values of resistors used in the design were selected to be compatible with hybrid process techniques. Insofar as possible, extremes in values, both high and low, were avoided during the detailed design phase of the effort. Also, the use of large values of capacitors were avoided, except for tantulum filters.

Three steps were taken in Phase III of the study to select candidate circuits for conversion into hybrid form. These steps were:

- The state of the art in hybrid technology, particularly the areas involving the use of power devices, was reviewed.
- The design for the power supply was analyzed and candidate circuits for conversion into hybrid form were selected.
- Preliminary design specifications for the selected circuits were prepared and reviewed with competent hybrid vendors to determine the feasibility of fabricating them.

P

5.1 REVIEW OF CURRENT HYBRID CIRCUIT TECHNOLOGY

The current level of technology involved in fabricating hybrid circuits was reviewed by discussing the subject with a number of vendors and by reviewing recent applicable publications. The results of the review showed the following requirements:

- The absolute tolerences on values of resistors used in a hybrid circuit should not be greater than ±5 percent. Plus or minus 10 percent was preferable to avoid trimming of components.

- The temperature coefficients of resistors should not be required to be less than 200 parts per million per degree centigrade (50 ppm/°C is obtainable at added cost).

- The absolute value of the capacitance of a capacitor should be less than approximately 0.02 microfarad (larger values can be obtained if tantalum capacitors are used).

- To be cost-effective, the capacitors should have tolerances and temperature coefficients limited to, typically, ± 5 percent and 200 parts per million per degree centigrade.

- To ensure cost-effectiveness, standard or preferred components, especially transistors and diodes, should be used.

- The power dissipation per square inch of hybrid substrate should be less than 5 watts.

With few exceptions, the design selected for the power supply meets these requirements.

5.2 SELECTION OF CANDIDATE HYBRID CIRCUITS

In selecting the candidate circuits for hybridization from the design, the following guidelines were used:

- The circuit selected should offer reasonable flexibility with regard to packaging.
- The circuit should be able to adapt to possible component improvements.
- Consideration should be given to grouping hybrid circuits into functional types such that their use will be flexible.
- The circuit selected should afford minimum size without jeopardizing maintainability or cost to repair.
- The circuit selected should enhance performance of the power supply; e.g., it should be compatible with good design practices and techniques.
- The circuit should enhance checkout at both the hybrid circuit level and the power supply unit level.

5.3 SELECTION OF THE HYBRID CANDIDATES

Using the guidelines listed in Section 5.2, the hybrid circuit candidates were selected. The approach, although simple, was primarily based on subdividing the electrical schematic of the power supply into usable, functional circuit blocks. These criteria were used, since it basically fulfills the basic guidelines established. The functional blocks selected were:

- Oscillator and control logic
- Preregulator and comparitor
- Regulator (start-up regulator), pre-driver, and driver
- Reference and summing amplifier
- Over-voltage and under-voltage detector.

(An overall schematic diagram and schematics of the selected hybrids are shown in Figures 5-1 through 5-5.) This division offers the following advantages:

- Each of the five circuits contains components which would require the same standard hybrid package size.
- The power stage is separated from the low-level circuitry.
- Each hybrid circuit is a complete functional block and can be tested easily and independently, greatly reducing the test and troubleshooting time required and, therefore, the cost.
- Five hybrids sufficiently subdivide the circuit such that the cost of each hybrid is low; therefore, maintenance costs are low.

5.4 REVIEW OF CANDIDATE HYBRID CIRCUITS

The candidate hybrid circuits were reviewed to eliminate those circuit elements that were either incompatible with hybrid techniques or that were to be eliminated from the hybrid as a result of performance requirements, e.g., the output voltage programming resistor, etc.

In addition to this review, a preliminary specification describing the hybrids was written. The specification included a list of discrete device and component types to be used in the hybrids, general component performance criteria, hybrid size and quality specifications, and areas of special attention such as transistor matching requirements, and active and passive component trimming requirements. This specification was sent to 17 qualified hybrid vendors for preliminary quotation. The responses to this preliminary quotation confirmed that the design was compatible with current hybrid techniques and that these hybrids could be produced at reasonable costs and within the size requirements specified.

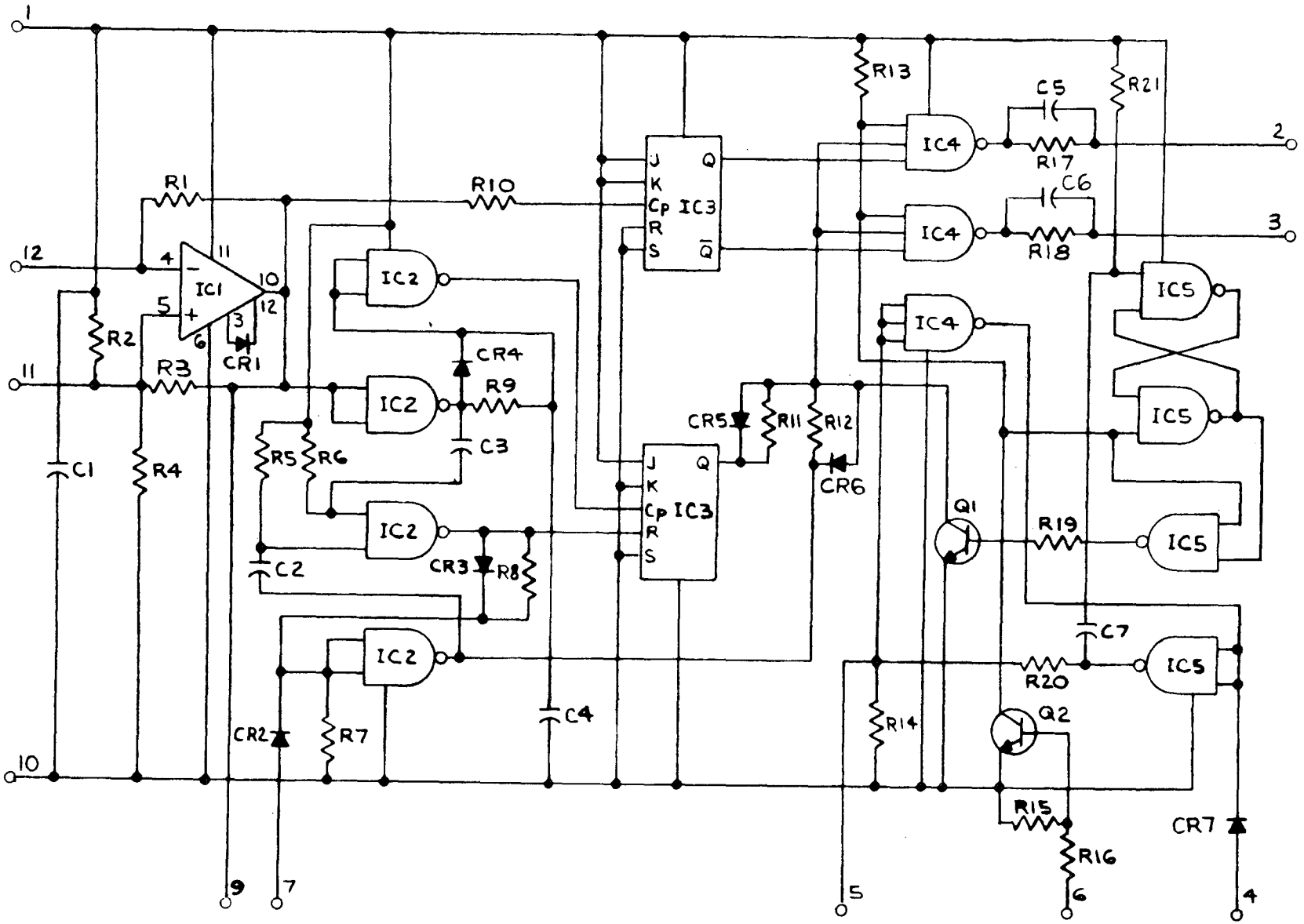

FIGURE 5-1. OSCILLATOR AND CONTROL LOGIC HYBRID INTEGRATED CIRCUIT

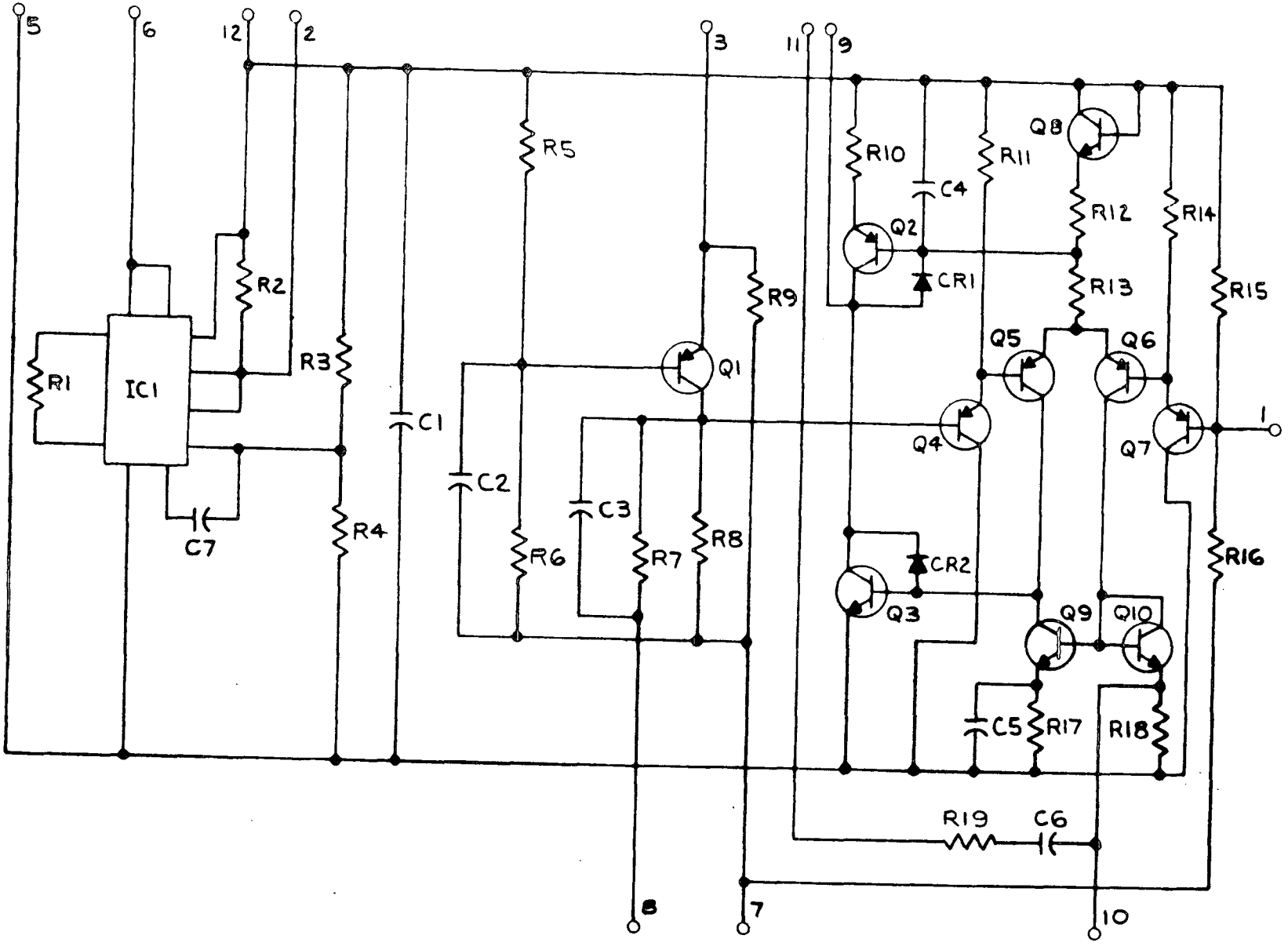

FIGURE 5-2. PREREGULATOR AND COMPARATOR HYBRID INTEGRATED CIRCUIT

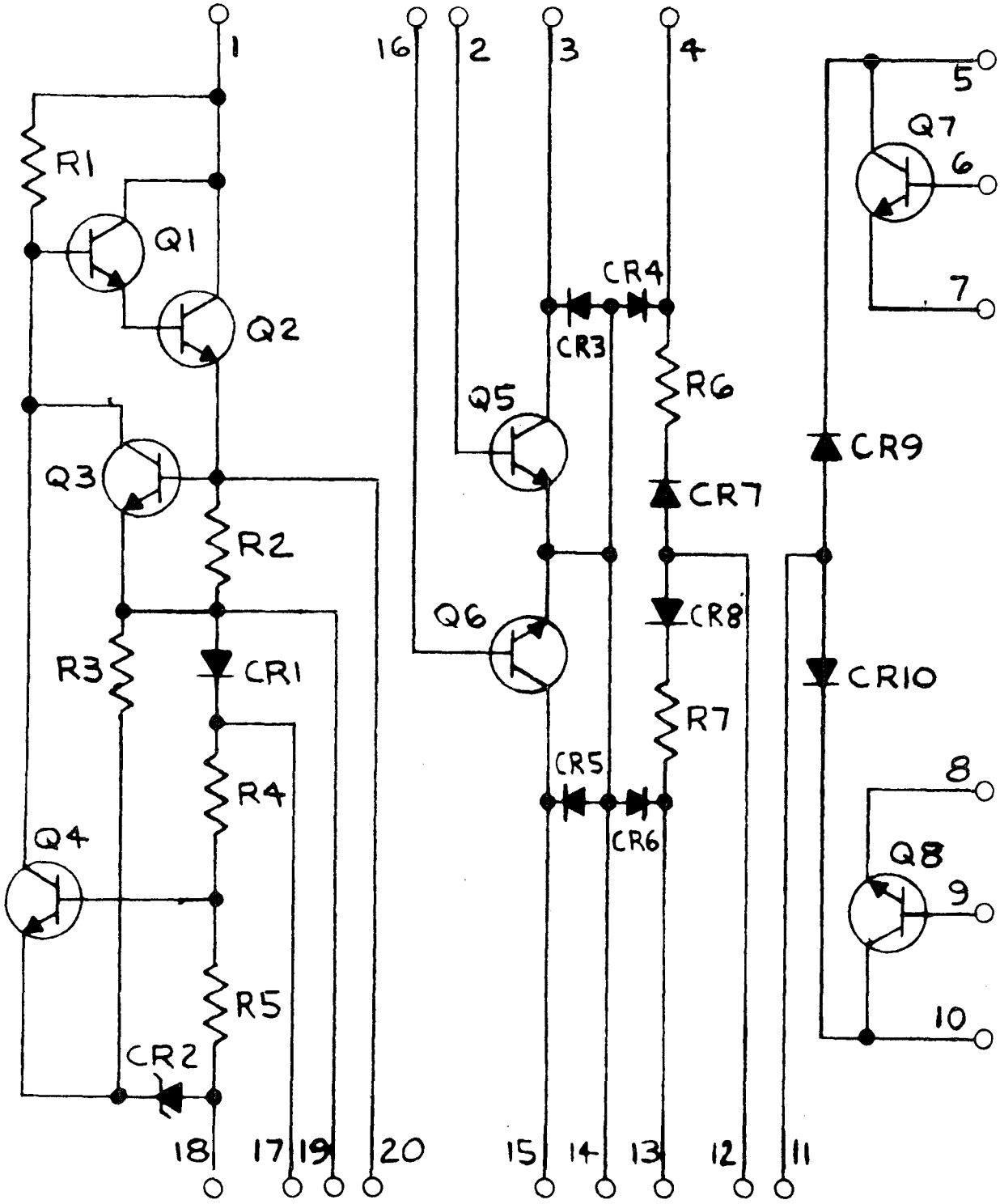

FIGURE 5-3. REGULATOR, PREDRIVER, AND DRIVER HYBRID INTEGRATED CIRCUIT

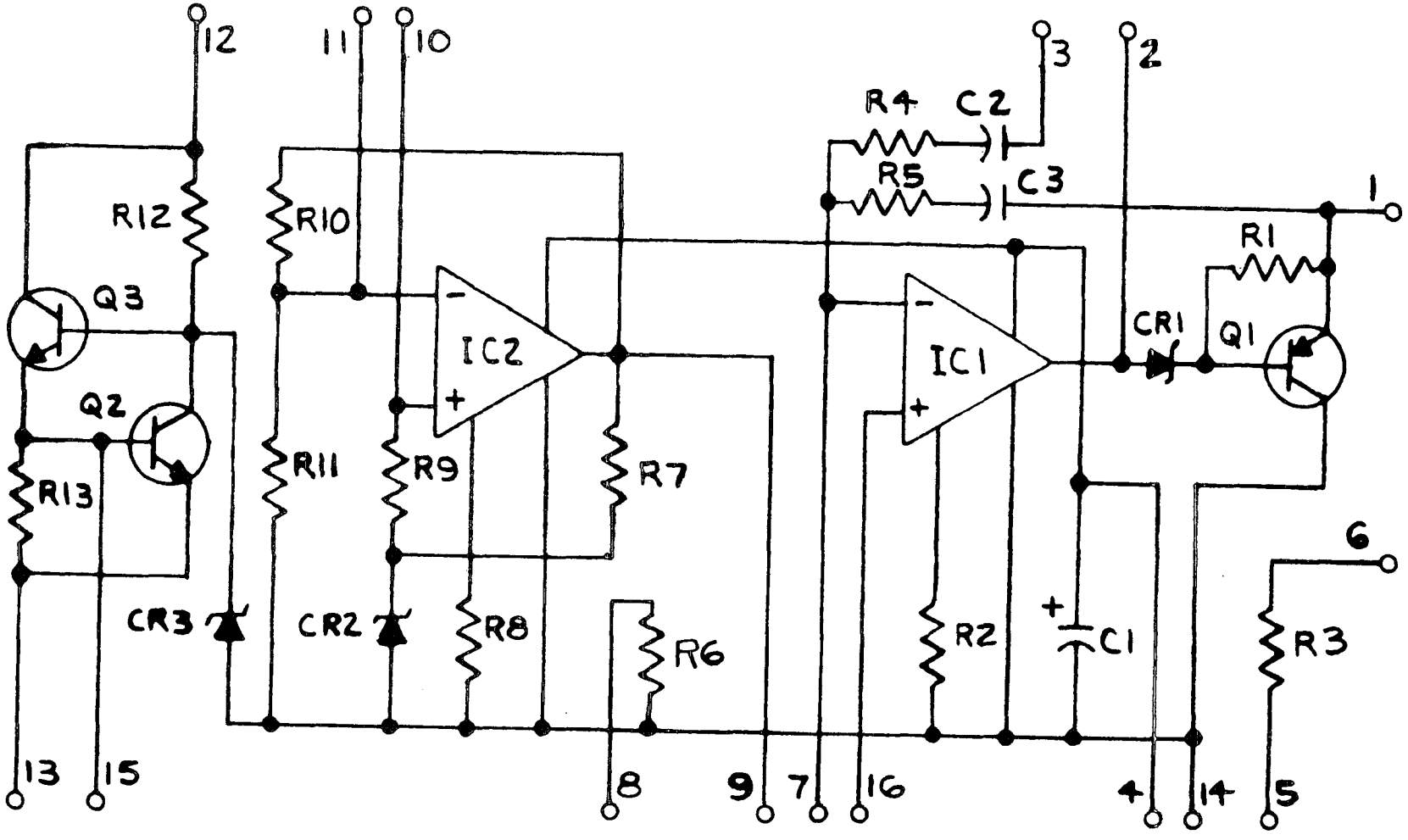

FIGURE 5-4. REFERENCE AND SUMMING AMPLIFIER

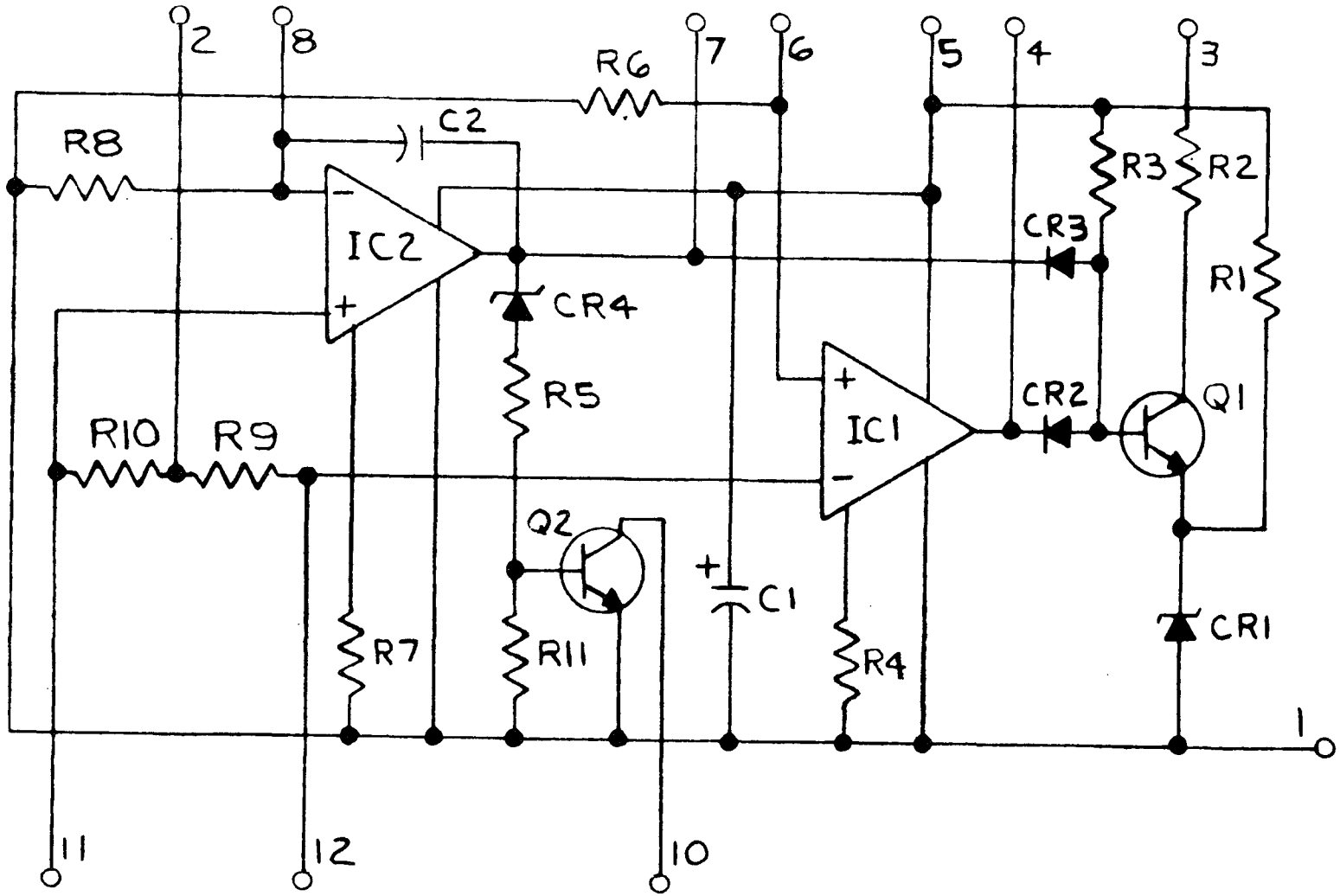

FIGURE 5-5. OVERVOLTAGE DETECTION AND UNDERVOLTAGE DETECTION HYBRID INTEGRATED CIRCUIT

6. PHASE IV ACTIVITIES AND ACCOMPLISHMENTS

During Phase IV of the study, a concept of packaging the power supply was developed, and details for housings, circuit boards, and other elements of the design were prepared. The package design utilizes modular construction which provides a high degree of flexibility, so that the power supply can be easily modified to meet changes in requirements for conditioned power.

A tradeoff study was performed during Phase I to establish the best overall package configuration for the optimum power supply. Three candidate configurations were evaluated to determine the relative cost, size, weight, maintainability, spares, logistics, and environmental performance of each when used in a power system such as that planned for the Space Shuttle or Manned Space Station.

Several guidelines for the packaging tradeoff study were established, based on the requirements for the programs which will use the power supply and the conclusions of the tradeoffs conducted during the first three phases of this study. These guidelines are summarized as follows:

- Equipment configuration - separate power supplies will be provided for each Line Replaceable Unit (LRU)
- Load power requirements - the maximum power output required for any LRU will be 150 watts
- Operating voltages - the maximum number of different voltages required for any LRU will be six.

6.1 PACKAGE DESIGN ASSUMPTIONS

The following paragraphs present the assumptions made to further define the packaging constraints for the standard power supply.

In general, these assumptions represent typical factors encountered in manned space vehicles. Whereas these assumptions may not be entirely correct for a particular system, such as for the Space Shuttle, they do contribute to the establishment of a baseline for this tradeoff study.

6.1.1 Sinusoidal Vibration

The power supply must operate as specified during exposure to the following sinusoidal vibration levels, in three mutually perpendicular axes (3 to 60 hertz at 3 octaves per minute):

- 3 to 6 hertz – 0.32 inch double amplitude displacement
- 6 to 10 hertz – 0.6 g peak
- 10 to 25 hertz – 0.11 inch double amplitude displacement
- 25 to 60 hertz – 3.6 g peak.

6.1.2 Random Vibration

The power supply must operate as specified during exposure to the following random vibration levels, in three mutually perpendicular axes (1 minute per axes):

- 20 hertz – 0.20 G^2/Hz
- 20 to 200 hertz – +3 dB/octave
- 200 to 700 hertz – 1.87 G^2/Hz
- 700 to 900 hertz – 18 dB/octave
- 900 to 2,000 hertz – 0.43 G^2/Hz.

6.1.3 Acoustical Noise

The power supply must operate as specified when exposed to a high-level noise environment of 142.5 decibels referenced to 2×10^{-5} N/m^2 for a period of 30 seconds, and to a low-level noise environment of 141.5 decibels referenced to 2×10^{-5} N/m^2 for 30 seconds.

6.1.4 Shock Criteria

The power supply must withstand and continue operating when exposed to the following shock spectrum (there are three shocks in each axis, nine shocks total):

- 12.5 to 20 hertz -- 5-g peak
- 20 to 250 hertz -- 44 dB/octave
- 250 to 320 hertz -- 27-g peak.

6.1.5 Humidity (Nonoperational)

The power supply must withstand exposure to a relative humidity of 100 percent.

6.1.6 Altitude

The power supply must not be damaged or its performance impaired by exposure to an altitude equivalent to 10^{-6} torr.

6.2 CANDIDATE PACKAGE CONFIGURATIONS

The three basic configurations listed below were evaluated for the optimum power supply:

- Custom designed, wherein the individual requirements of each LRU are established and a custom designed assembly is created
- Modular family system, wherein standard modules of the various operating voltage and power levels are available for custom assembly to meet the individual LRU requirements
- Subsystem modules, wherein subsystem elements (converter, output rectifier and filter, input filter, etc.) will be prepackaged and documented for inclusion in the individual LRU assembly.

6.3 PACKAGE DESIGN TRADEOFF STUDY

A packaging tradeoff study was performed and the following parameters evaluated:

- Cost
- Weight
- Size and complexity.

These parameters obviously are not the only factors which will influence the selection of the package configuration for the standard power supply. For example, maintainability and logistics support are two very important factors. However, these considerations and certain others do not lend themselves to direct comparison between the candidate configurations. They will be discussed in some detail later in this section.

6.3.1 Cost Considerations

For the purpose of this discussion, detailed cost estimates of the candidate configurations were not made. However, relative costs are readily apparent and easily estimated.

Component costs for the three configurations will be identical except for the subsystem connectors required in the two modular approaches. The differences in cost for the three configurations are in the areas of

- Nonrecurring design and documentation
- Mechanical parts, such as module housings, shielding, etc.
- Cost of one-of-a-kind fabrication as compared with multiple-usage quantity fabrication.

Design and documentation costs for the custom power supply approach would consist of preliminary design to standardize as much as possible, and detailed design for every LRU application. Assuming 160 man-hours for this detail design and using the 134 LRUs indicated in preliminary Shuttle reports, the design and documentation effort would require approximately 21,400 man-hours. Conservative estimates on

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the nonrecurring costs for the two modular approaches indicate an order of magnitude reduction would be possible in design and documentation man-hours.

Use of custom power supply approach would result in the minimum amount of mechanical parts. The two modular approaches would require additional housings and mounting hardware. However, part of the additional cost involved in the extra housings would be required in the custom design concept in the form of shielding between the various elements. Based on past experience, the mechanical costs for a power supply are approximately 30 percent of the total fabrication and material costs. Assuming a 50-percent increase in mechanical costs, the overall price increase for the total package would be 15 percent. The cost increase for the subsystem module approach would be somewhat less, since an overall housing would not be required; however, additional fabrication costs of the individual LRUs would probably offset this savings.

In the area of relative costs between one-of-a-kind and multiple-usage fabrication, it is difficult to determine the actual cost differential. Intuitively, costs for quantity fabrication will be significantly less. However, a certain amount of standardization will be possible in the custom design approach, approximately 50 percent. Since the quantity of power supplies is unknown at this time, additional difficulty is encountered in assessing the relative costs. Based on the 134 potential users identified in Space Shuttle application, it is estimated that the two modular approaches would have approximately a 25-percent reduction in fabrication costs.

From this discussion, it can be stated that either of the two modular approaches offers significant cost advantages over the custom

design. Taking into account the added cost to the user in the subsystem module approach, the two modular configurations are approximately equal.

6.3.2 Weight Considerations

Since the component complements for the three approaches are the same, the differences in weight are in the areas of mechanical design of the module and overall housings. The subsystem modular approach will be the lightest, since it will not require an overall housing and, in many instances, will not require shielding against electromagnetic interference and radio frequency interference (EMI/RFI). The modular family system will weigh the most, with the custom design approximately midway between the two extremes.

Whereas weight is always important in any space-flight application, it should be noted that the worst-case configuration, i.e., modular family configuration with six different output voltages and full EMI/RFI filtering, will weigh less than 40 pounds.

6.3.3 Size and Complexity

A review of state-of-the-art power systems indicates that the customer-designed power supply could be packaged in a volume of 1 in^3/W; thus, a 150-watt supply with one output voltage would require approximately 150 in^3, excluding flight connectors. The modular family approach would require 350 to 400 in^3, or approximately 2.7 in^3/W. The subsystem modular approach would have 250 to 300 in^3; however, the extra volume needed in the individual LRUs will make the volume required approximately the same as for the other modular approach.

The complexity of the three systems is roughly equal. For six different voltage levels at three separate power levels with a 150-watt maximum power output, 58,078 possible combinations are available to the user. This number of combinations does not take into account the

±20 percent deviation from the nominal voltage that is programmable for each output.

Complexity of this magnitude is never easy to control; however, the two modular approaches using conventional tabulating techniques offer tremendous advantages over the custom-design configuration.

6.3.4 Other Considerations

Environmental performance of the three configurations can be accomplished with approximately the same effort, and, although it is always important, it is not a factor in this tradeoff analysis.

Although the maintenance concept for future space-flight applications has not been defined, the circuit design offers built-in failure indication and fault isolation which would allow limited in-flight repair and replacement. The modular configurations will allow replacement at a lower level than the custom-design approach.

Spares logistic requirements would be considerably lower in the modular approaches since interchangeability between modules would allow one module to serve as back-up for several LRU power supplies.

Reliability of the three configurations will be approximately the same. However, some form of reliability demonstration testing will be required for each custom design, whereas the different configurations of the modular approaches could be flight qualified by similarity.

6.3.5 Conclusions

The advantages of size and weight offered by the custom-design approach are more than offset by the significant cost savings possible in the modular configurations.

Since no significant differences exist in the two modular approaches, this study recommends that the optimum power supply be designed in the modular family configuration and that the modules should be sufficiently

self-contained to be incorporated in the individual LRU packages, if desired.

6.4 PACKAGE DESIGN DESCRIPTION

Figure 6-1 shows the preliminary design concept that has been selected for the standard power supply. The design shown in this figure is for one of the more than 58,000 combinations of arrangements possible for the power supply. The configuration shown contains the following output voltages:

- 24 to 36 volts, 50 watts
- 4 to 6 volts, 25 watts
- 12 to 18 volts, 25 watts
- 12 to 18 volts, 10 watts
- 36 to 54 volts, 10 watts
- 72 to 108 volts, 10 watts.

6.4.1 Overall Package Description

The power supply design consists of a wraparound, formed, and welded outer housing, a removable wiring plane, top and bottom covers, 13 modules, and RFI feedthrough capacitors, filters, and gaskets.

The wiring plane, when assembled to the outer housing, contains mating connectors for the various modules, brackets for thermal transfer to the bottom, cover/mating plate, and all the necessary feedthrough capacitors and filters, and provides a rigid mounting surface for the modules. It also forms two separate, isolated RFI cavities for the input and output connectors. The design features of the subsystem modules will be discussed in the following section.

6.4.2 Individual Module Description

The elementary schematic for the optimum power supply is shown in Figure 6-2. As indicated in the schematic, the power supply has been divided into three separate modules. The modules and their configurations are:

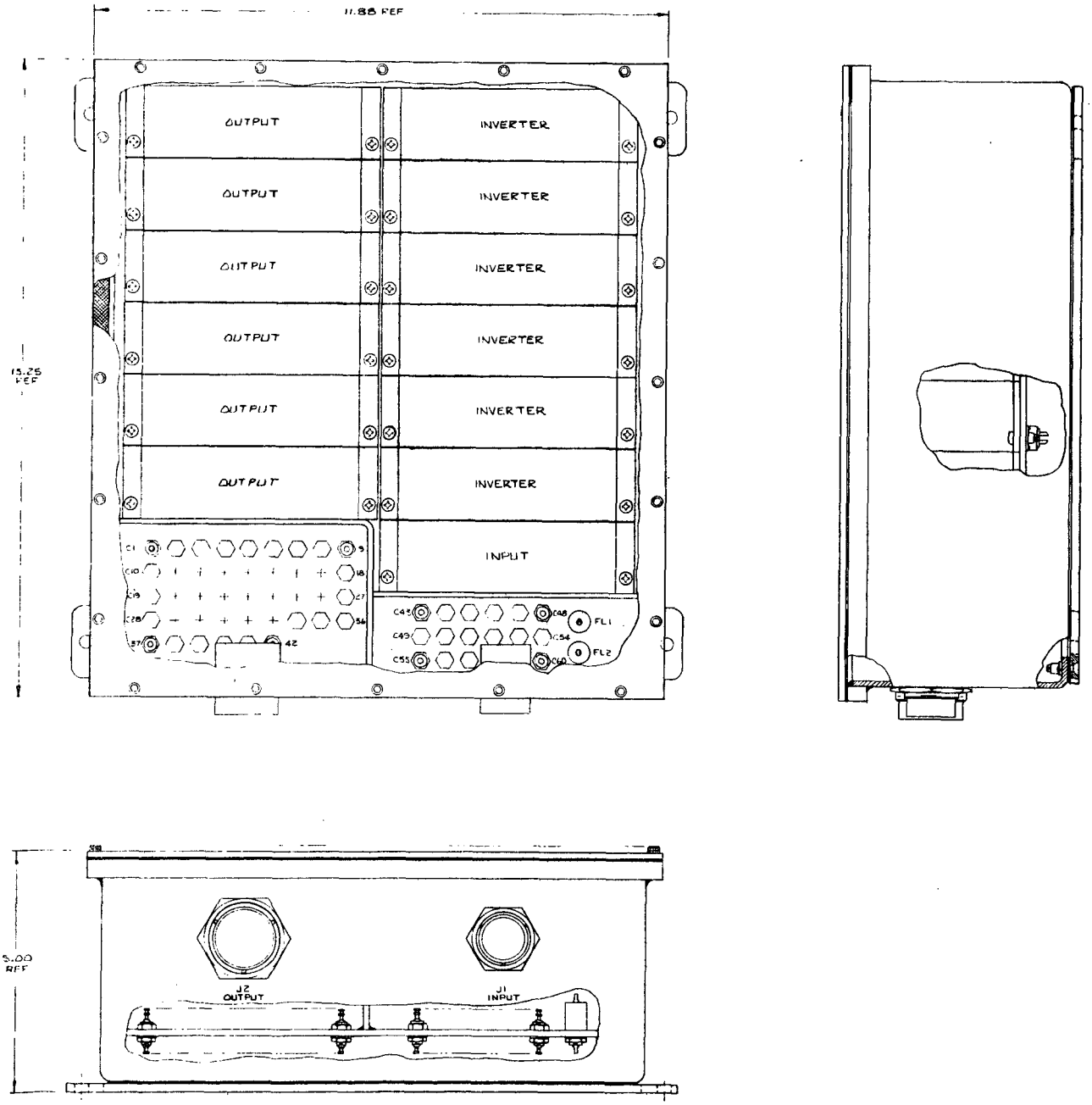


FIGURE 6-1. TYPICAL OVERALL PACKAGE ASSEMBLY

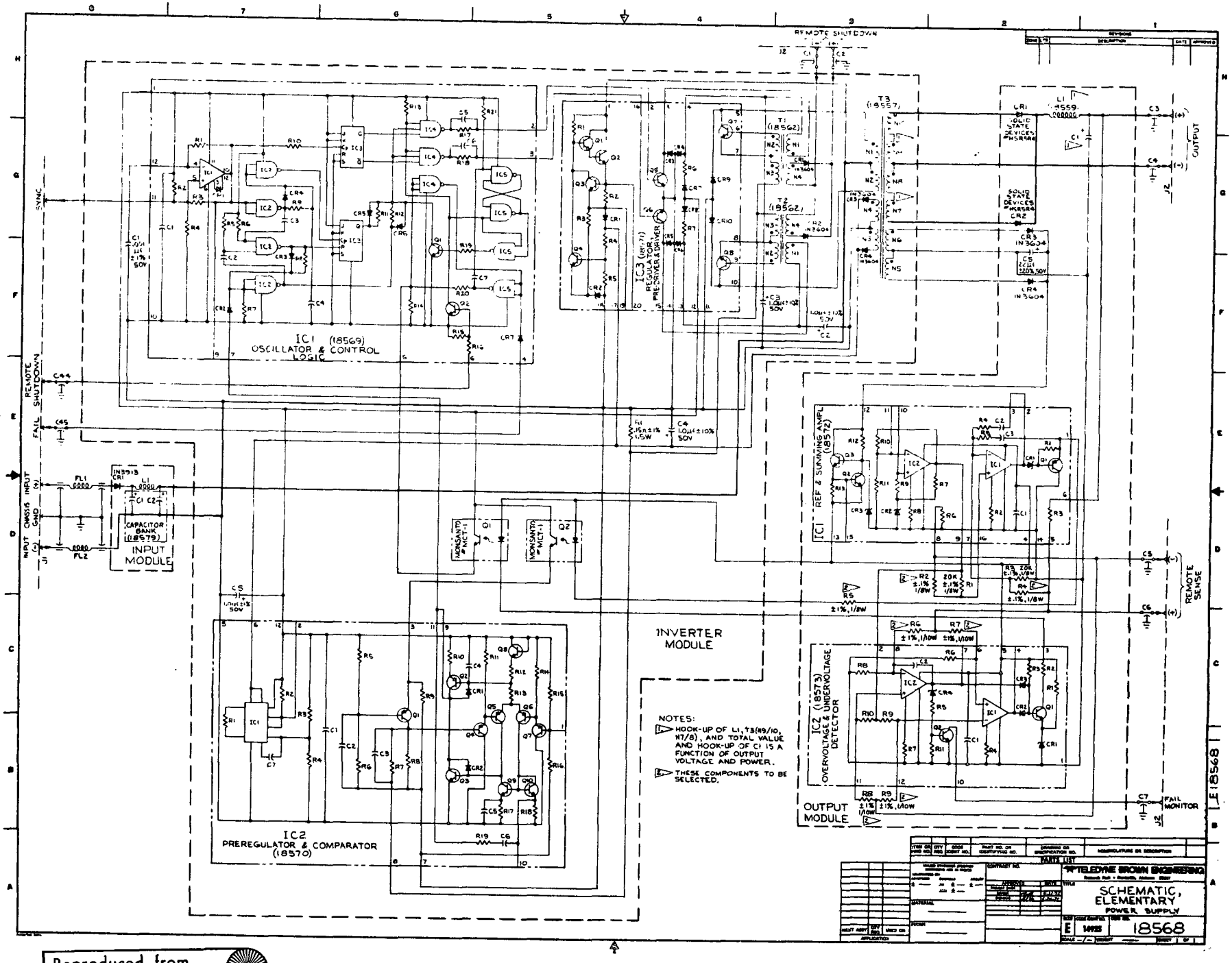


FIGURE 6-2. OVERALL SCHEMATIC DIAGRAM

- Input Filter -- available in 50-, 100-, or 150-watt versions

- Inverter -- 10-, 25-, and 50-watt and 5-, 10-, 15-, 30-, 45-, and 90-volt configurations for each power level

- Output -- 10-, 25-, and 50-watt outputs with 5-, 10-, 15-, 30-, 45-, and 90-volt (±10%) nominal voltage ranges for each power level.

The modules are completely self-contained in a machined aluminum alloy housing. Interface connectors are provided to allow assembly into separate power supplies, or for inclusion in the individual LRU packages.

6.4.2.1 Input Module - The input module, shown in Figure 6-3, consists of a capacitor module (an encapsulated printed circuit cordwood module), toroidal inductors which are encapsulated and hard-mounted to the machined aluminum housing, a stud-mounted diode, and the interface connector.

6.4.2.2 Inverter Module - The inverter module, shown in Figure 6-4, consists of a machined aluminum housing containing the power transformer, a printed circuit assembly, and the interface connector. The power transformer is a toroid, encapsulated in a mu-metal shield and hard-mounted to the module housing. The printed circuit assembly is a double-sided, plated-through hole circuit board with components mounted on both sides. The circuit board contains the two pot-core-drive transformers, three integrated circuits, and the remaining discrete components. The printed circuit assembly is mounted such that the integrated circuit containing the regulator, pre-driver, and driver contacts the module housing to assure adequate thermal conductivity. The variables required in the inverter module to obtain the different power levels and voltage ranges are associated only with the output transformer and its connection.

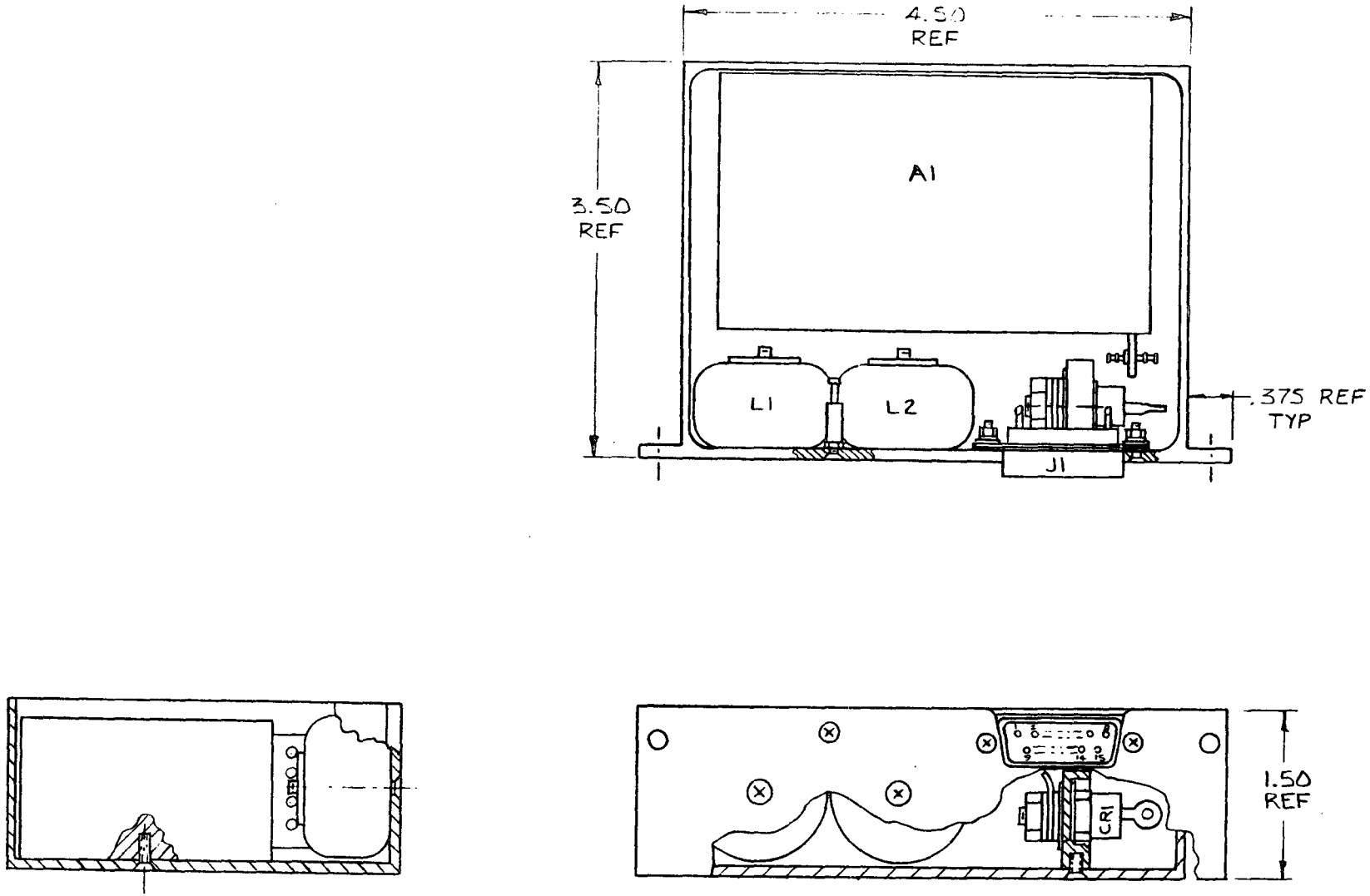


FIGURE 6-3. INPUT MODULE ASSEMBLY

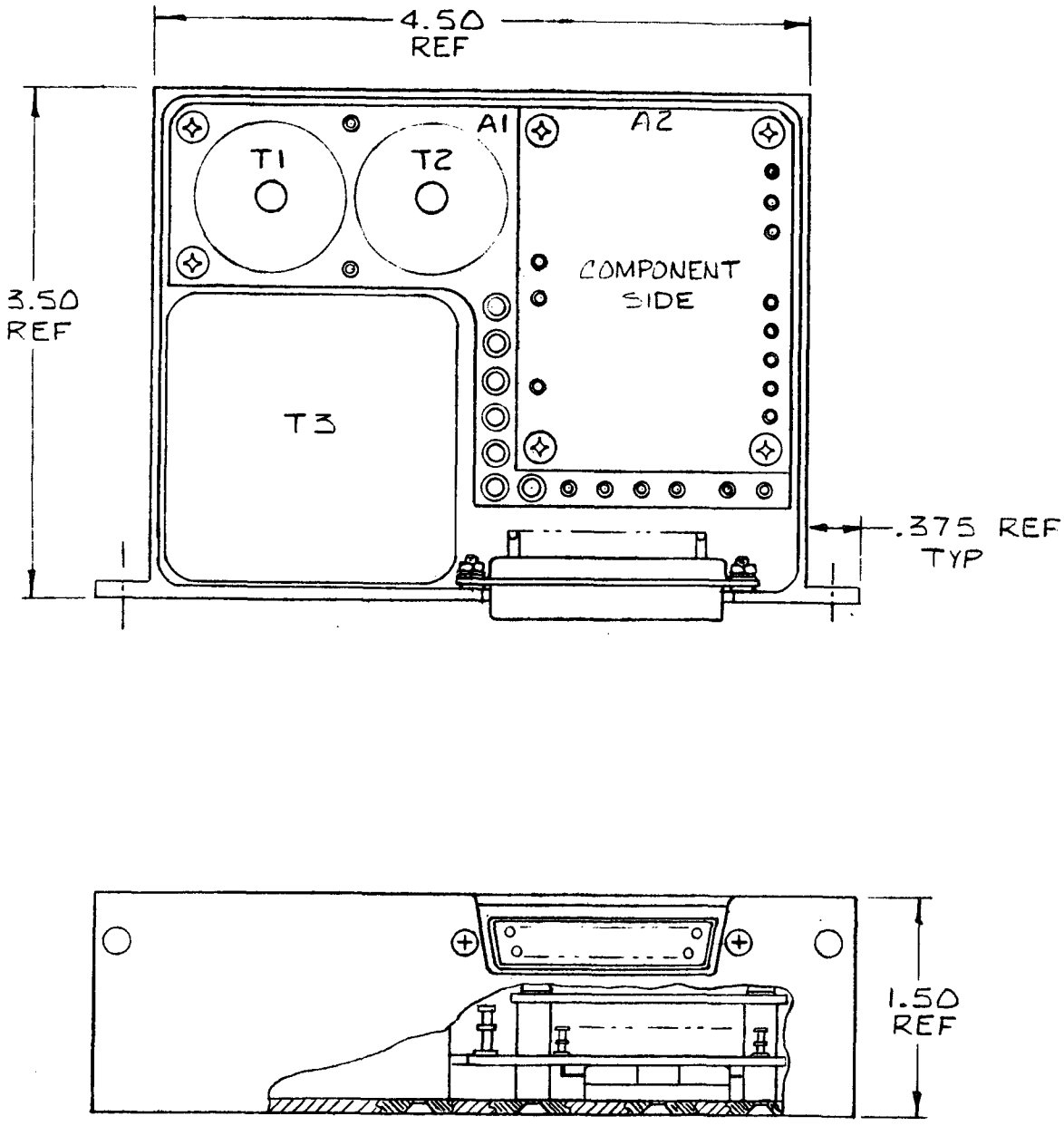


FIGURE 6-4. INVERTER MODULE ASSEMBLY

6.4.2.3 Output Module - The output module, shown in Figure 6-5, consists of a machined aluminum housing containing the rectifiers, the output filter, a printed circuit assembly, and an interface connector. The printed circuit board contains two integrated circuits, various discrete components, and easily accessible terminals for mounting and terminating the test select resistors. The filter inductor is an encapsulated toroid that is hard-mounted to the housing of the module.

6.4.3 Documentation

The drawing package contains the indentured assembly-level generation breakdown of the documentation generated as a result of this study. The generation breakdown also indicates the status of the various drawings: final working drawing, preliminary drawings, or to be determined. The documentation has not been finalized because of a lack of form-factor definition on the integrated circuits. In general, the magnetic components and input filter modules are final and the two modules containing integrated circuits are preliminary since form-factor changes probably would result in changes up through the printed circuit assemblies and module housings.

6.4.4 Typical Configurations

Figure 6-6 shows the 56 possible combinations of output power-level configurations that are available. Using the expression

$$\frac{(N + K - 1)!}{K!\,(N - 1)!}$$

to determine the combinations of N different items (K) at a time with repetitions, the total combinations of voltage levels within a voltage rating can be calculated. Multiplying these numbers together for each of the 56 power-level combinations and adding the products shows 58,078 possible combinations.

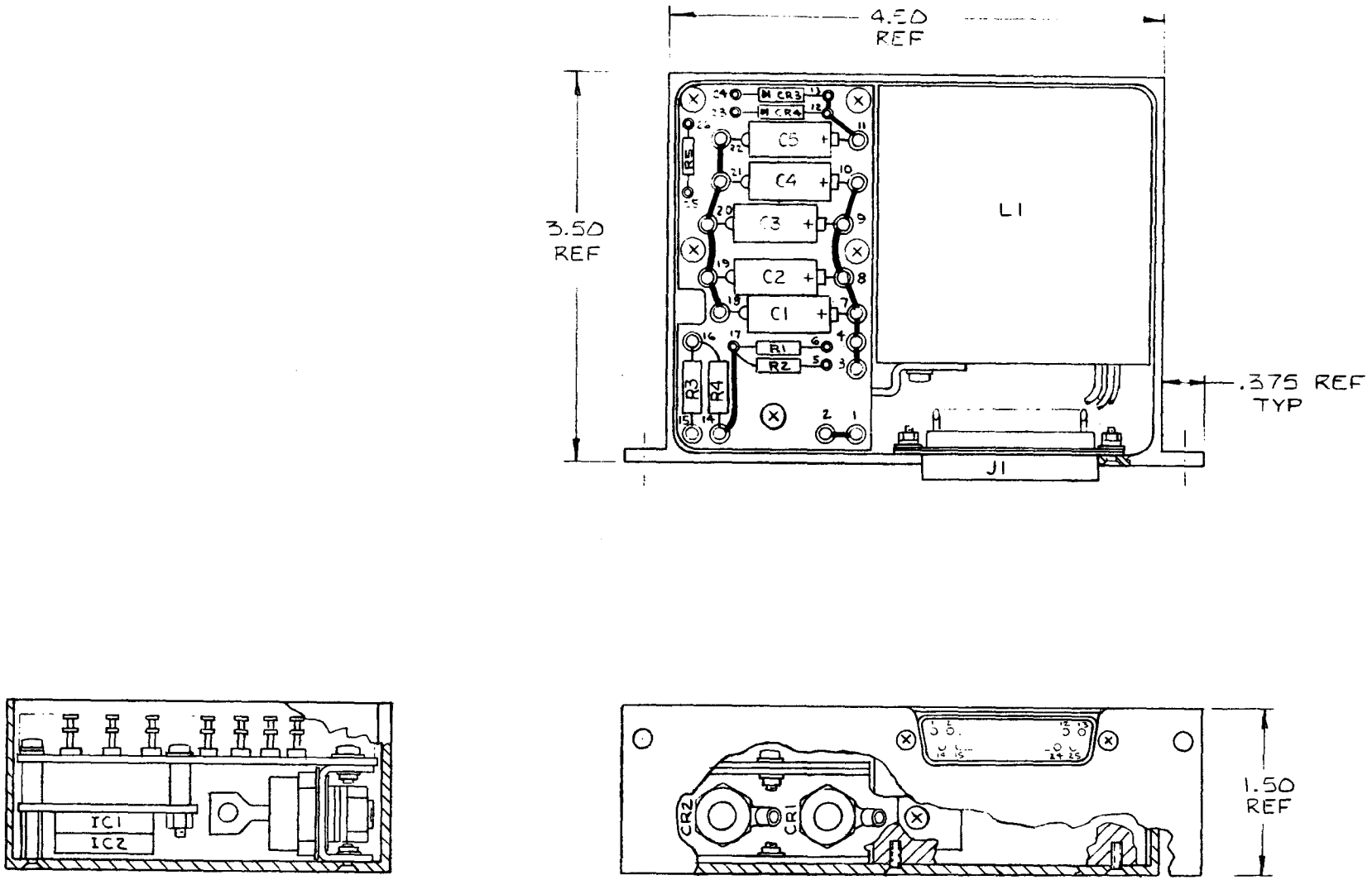


FIGURE 6-5. OUTPUT MODULE ASSEMBLY

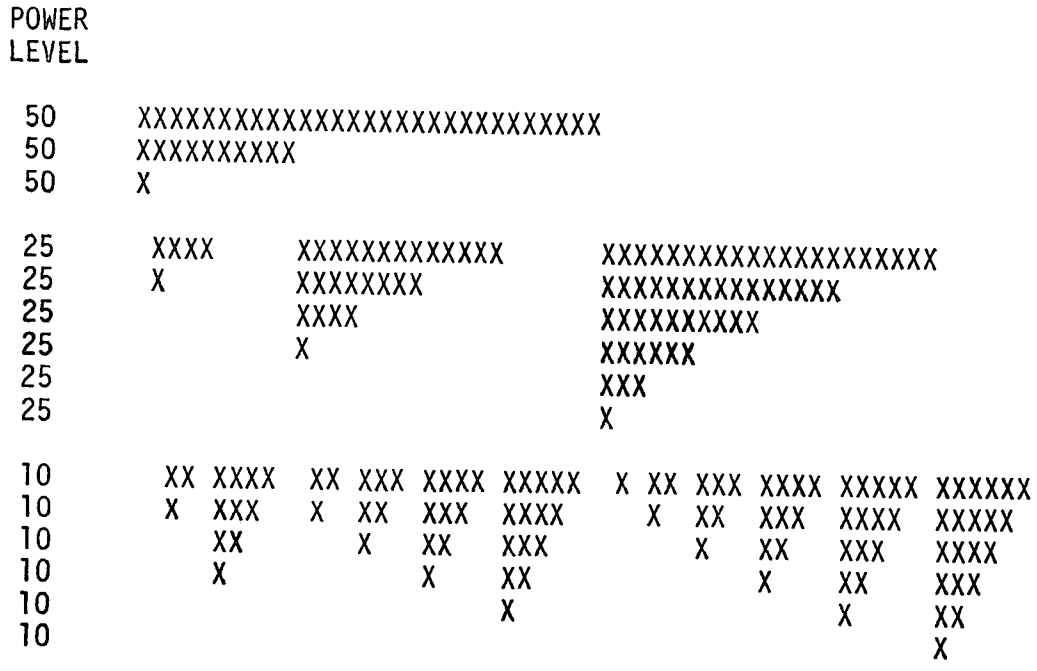


FIGURE 6-6. OUTPUT POWER-LEVEL COMBINATIONS FOR THE POWER SUPPLY

The 58,078 number was determined on the basis of the six standard voltages available. When the ±20 percent variation in output voltage that is available by changing test select resistor values is considered, the total number of available combinations is astronomical.

6.5 THERMAL ANALYSIS FOR THE POWER SUPPLY

Because of the high conversion efficiency of this power supply and the very few localized "hot spots", an extensive thermal design was not required. Therefore, the basic thermal analysis for the power supply was limited to a simple description of a typical thermal situation.

For purposes of the analysis, an absolute maximum, worst-case power loss was calculated; however, this power loss will never be encountered. The worst-case power-loss situations considered included power losses caused by internal failures and worst-case temperature extremes, and the sum of all the maximum losses. For example, the power loss for the filter capacitors was calculated as the sum of the ripple current power loss at -20°C and the leakage current power loss at 125°C.

The worst-case power losses in each module are:

- Input Filter Module (150-watt): 4.24 watts lost
  (Dimensions: 4.5 by 3.5 by 1.5 in.)
- Converter (50-watt): 7.26 watts lost
  (Dimensions: 4.5 by 3.5 by 1.5 in.)
- Output Filter (50-watt, 5-volt): 5.92 watts lost
  (Dimensions: 4.5 by 3.5 by 1.5 in.)

Therefore, the total absolute maximum power loss for a 150-watt, 5-volt, 30-ampere supply is 43.77 watts (dimensions of 5 by 8 by 11 inches). The base plate of the power supply was assumed to be mounted to an infinite heat sink, at +85°C. Seven aluminum heat shunts will be mounted under the module to the base plate. These shunts will connect the outside

surface with the mounting flange of the module. The shunts are 0.75 inch thick, 1.25 inch high, and 4 inches long. For an approximation of the thermal resistance, a uniform heat source with seven parallel paths was considered. This is justified because the mounting plate of the actual power supply module will spread the heat, and each module will have approximately the same amount of power loss.

An analogous system is shown in Figure 6-7. An individual heat path for this model is shown schematically in Figure 6-8. Calculations are as follows:

$$\theta = \frac{t}{A\,K}$$

where

θ - thermal resistance

t - thermal path length

A - thermal path area

K - thermal conductivity.

The following assumption was made:

Interface thermal resistance = $(0.3°C\text{-}cm^2)/W$ per square centimeter of mounting area.

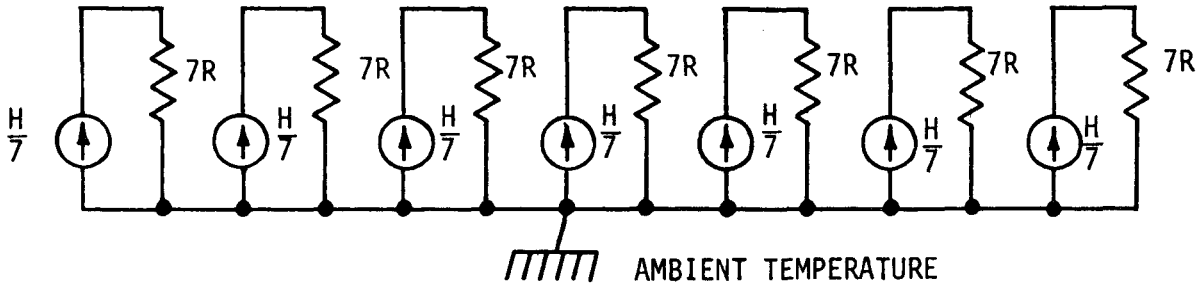
Typical values for each thermal resistance shown in Figure 6-8 are as follows:

$$\theta_{mp} = [(0.3°C\text{-}cm^2)/W]\ [1/(3.8 \times 11.4)]$$

$$\theta_{mp} = 0.007°C/W \quad .$$

$$\theta_p = \frac{0.318\ cm}{(42.5\ cm^2)\ [0.475\ cal/(sec\text{-}cm\text{-}°C)]}$$

$$\theta_p = 0.0156\ °C/W \quad .$$



H - TOTAL HEAT
R - TOTAL THERMAL RESISTANCE

FIGURE 6-7. THERMAL MODEL FOR COMPLETE POWER SUPPLY

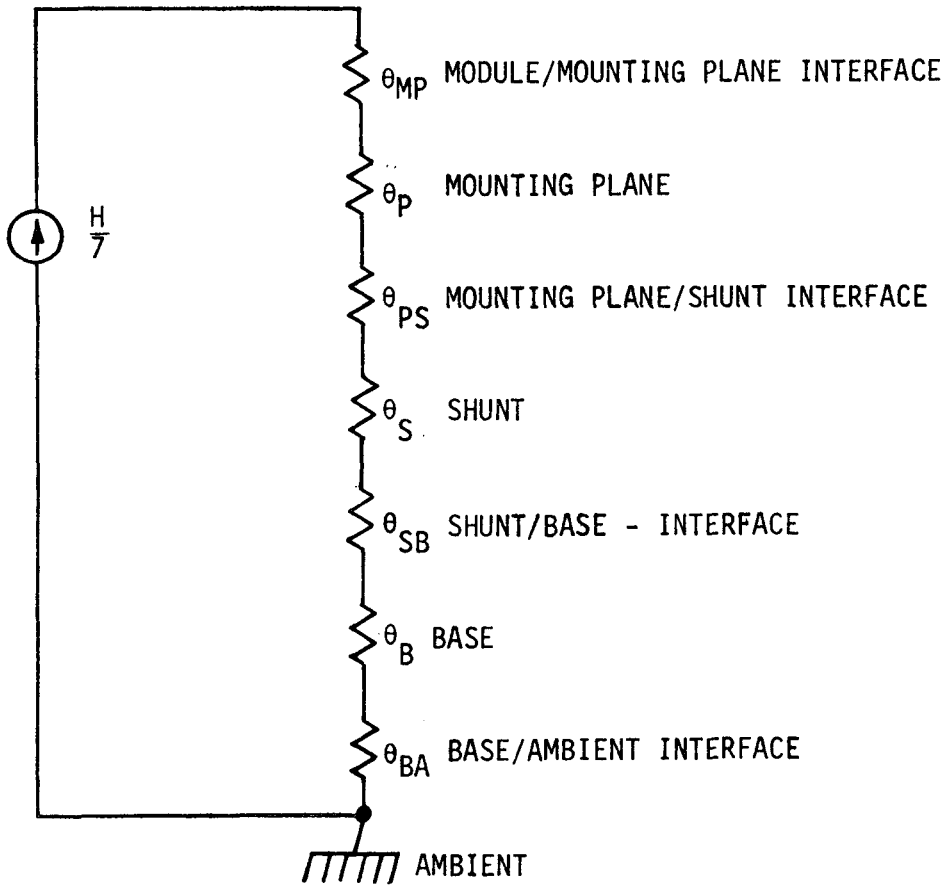


FIGURE 6-8. INDIVIDUAL COMPONENT OF THERMAL MODEL

$$\theta_{ps} = 0.007°C/W \quad .$$

$$\theta_s = \frac{3.2 \text{ cm}}{(42.5 \text{ cm}^2)\,[0.475 \text{ cal}/(\text{sec-cm-}°C)]}$$

$$\theta_s = 0.158°C/W \quad .$$

$$\theta_{sb} = 0.007°C/W \quad .$$

$$\theta_b = \frac{0.52 \text{ cm}}{(42.5 \text{ cm}^2)\,[0.475 \text{ cal}/(\text{sec-cm-}°C)]}$$

$$\theta_b = 0.025°C/W \quad .$$

$$\theta_{ba} = 0.007°C/W \quad .$$

The total thermal resistance from the module to the ambient temperature plane is

$$R_{ma} = \theta_{mp} + \theta_p + \theta_{ps} + \theta_s + \theta_{sb} + \theta_b + \theta_{ba}$$

$$R_{ma} = 0.227°C/W$$

and the total equivalent thermal resistance is

$$(0.227°C/W)\,(1/7) = 0.0325°C/W \quad .$$

The temperature at the module mounting plate was determined as follows:

$$T_{mounting} = (0.227°C/W)\,(43.77\ W/7) = 1.42°C \text{ rise} \quad .$$

6.5.1 Input Filter Module Temperature Rise

The temperature rise inside the input filter modules was calculated as follows (assuming a suitable potting compound is used):

Area of the capacitor bank $\approx$ (10 cm) (5.8 cm) = 58 cm

Average thickness of potting compound = 1 cm

Thermal conductivity of the potting compound = 0.001 cal/(sec-cm-°C) .

Therefore,

$$\theta = \frac{1 \text{ cm}}{(58)(0.001)} = 17°\text{C/W}$$

Capacitor temperature rise = (17°C/W) (1.24 W loss)

= 21°C above the flange temperature.

The temperature rise inside the inductors was calculated as follows:

Power loss = 0.45 W

Area = 20 cm

Compound thickness = 1 cm .

Therefore

$$\theta = \frac{1}{(20)(0.001)} = 40°C/W$$

and

$$\text{Temperature rise} = (40°C/W)(0.45\ W) = 18°C\ .$$

For the diodes, the following calculations were made:

$$\theta_T = \theta_{JC} + \theta_{CB} + \theta_B + \theta_{BF}$$

where

θ_T - total resistance

θ_{JC} - diode junction to case

θ_{CB} - case to bracket

θ_B - bracket

θ_{BF} - bracket to flange.

$$\theta_{JC} = 2.5°C/W$$

$$\theta_{CB} = \left(\frac{0.3°C - cm^2}{W}\right)(1\ cm) = 0.3°C/W$$

$$\theta_B = \frac{2\ cm}{(3\ cm)(0.475)} = 1.4°C/W$$

$$\theta_{BF} = \left(\frac{0.3°C - cm^2}{W}\right)\left(\frac{1}{3\ cm^2}\right) = 0.1°C/W$$

Therefore

$$\theta_T = 4.3°C/W$$

$$\text{Junction rise} = (4.3°C/W)(2.1\ W)$$

$$\text{Temperature rise} = 9°C\ .$$

6.5.2 Inverter Package Temperature Rise

In the inverter package, hybrid integrated circuit "C" dissipates 6.072 watts out of a total of 7.26 watts for the package. This will be considered the only significant heat source for the inverter package, and all others will assume a case temperature of 95°C, which will be well within their capabilities.

The calculation of hybrid "C" thermal resistance is as follows:

$$\theta_T = \theta_{JS} + \theta_S + \theta_{SC} + \theta_C + \theta_{CF} + \theta_{FMP}$$

where

θ_T - total resistance

θ_{JS} - junction to substrate

θ_S - substrate

θ_{SC} - substrate to case

θ_C - case

θ_{CF} - case to flange

θ_{FMP} - flange to mounting plate .

It is assumed that the junctions will lie on an aluminum substrate, epoxied to a kovar case and bolted to the mounting flange. With

$$\theta_{JS} = 2.5°C/W \text{ typical}$$

$$\theta_{S} = 3°C/W \text{ typical}$$

$$\theta_{SC} = 0.5°C/W \text{ typical}$$

$$\theta_{C} = 0.1°C/W \text{ typical}$$

$$\theta_{CF} = 0.5°C/W \text{ typical}$$

$$t = 5 \text{ cm}$$

$$A = (11.5)(0.25 \text{ cm}) ,$$

then

$$\theta_{FMP} = \frac{5}{(11.5)(0.25)(0.475)} = 3.65°C/W$$

Hybrid "C" case temperature rise = $(3.65°C/W)(6.07)$

$$= 22°C .$$

Assuming a maximum of 1.6 watts dissipated by any one device in the package, the junction temperature is

$$T_J = 86.4° + 22°C + (6.6°C/W)(1.6 W) = 118.9°C .$$

6.5.3 Output Filter Module Temperature Rise

The inductor case temperature is calculated as follows:

$$\text{Power loss} = 0.3 \text{ W}$$

$$\text{Area} = 36 \text{ cm}$$

$$\text{Path} = 2 \text{ cm}$$

$$\text{Case temperature rise} = \frac{(2 \text{ cm})(0.3 \text{ W})}{(36 \text{ cm}^2)\ [0.001 \text{ cal}/(\text{sec-cm-}^\circ\text{C})]}$$

$$= 1.6^\circ\text{C} \ .$$

Calculations for the diodes are given below:

$$\theta_T = \theta_{JC} + \theta_{CB} + \theta_B + \theta_{BF}$$

where

θ_{JC} - junction to case

θ_{CB} - case to bracket

θ_B - bracket

θ_{BF} - bracket to flange .

$$\theta_{JC} = 0.75^\circ\text{C/W}$$

$$\theta_{CB} = 0.2^\circ\text{C/W}$$

$$\theta_B = \frac{2 \text{ cm}}{(5 \text{ cm})(0.15)(0.45)} = 5.6^\circ\text{C/W}$$

$$\theta_{BF} = [(0.3°C - cm^2)/W] [1/(5\ cm^2)] = 0.06°C/W$$

$$\theta_T = [(6.61°C)/W] (5\ W) = 33°C$$

Diode junction temperature = 119.4°C .

TABLE 6-1. SUMMARY OF THERMAL ANALYSIS

ITEM	TEMPERATURE (°C)
Base Mounting Plate Temperature	85
Module Mounting Flange	86.4
Estimated Maximum Air Temperature	90
Input Filter Assembly	
Inductor Case	104.4
Capacitor Case	107.4
Diode Junction	95.4
Estimated Air Temperature	90
Inverter Assembly	
Hybrid "C" Case	108.4
Hybrid "C" Junction	118.9
Estimated Air Temperature	95
Output Filter Assembly	
Inductor Case	88
Diode Junction	119.4
Estimated Air Temperature	95

These figures represent the worst-case absolute maximum temperature rise.

The typical power supply will have less than one-half of these temperature rises.

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7. CONCLUSIONS AND RECOMMENDATIONS

7.1 CONCLUSIONS

This study effort has shown that a standard design configuration for a universal power supply, or power conditioner, would fulfill the needs of a high percentage of the power users in future manned aerospace programs. This optimized standard design can provide a significant reduction in cost and weight and an increase in reliability and performance for large aerospace vehicles. A design for a power supply which can fulfill these requirements is well within the present state of the art.

The use of hybrid integrated circuits in the design of the standard power supply results in a substantial reduction in the size and weight of the unit. Hybrid circuits can be used to perform a large percentage of the functions involved in the power supply.

A modular packaging concept for the power supply provides maximum flexibility in adapting the unit to various applications. The number of modules required to implement a design for a particular requirement can become quite large, but proper documentation techniques can be used to maintain control of the configurations.

7.2 RECOMMENDATIONS

The results of the study effort presented in this report indicate that an optimum, standard design is practical for airborne power supplies. The work performed to date has been based on analytical calculations and breadboard results. It is recommended that a nonflight prototype of a power supply similar to that discussed in the report be fabricated and tested using the concepts and designs documented herein. This prototype will prove to be of considerable value in establishing the standard power supply design as a viable concept for future aerospace programs.

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APPENDIX A. DESIGN SPECIFICATION FOR THE POWER SUPPLY

This appendix contains the preliminary design specification for the power supply. This specification is the result of the studies which were performed and the decisions which were reached in Phases I and II of the study effort.

DESIGN SPECIFICATION FOR A POWER CONDITIONER FOR MANNED SPACECRAFT

SCOPE

This specification establishes the requirements for power supplies that will be utilized in manned space vehicles. These power supplies will furnish conditioned, regulated dc power to various subassemblies which perform a number of critical functions during a flight mission. The subassemblies are defined herein as Line Replaceable Units (LRUs). The power supplies shall provide highly reliable performance under severe operating conditions. In addition, the supplies shall interface with the vehicle power distribution system, and other on-board subsystems which monitor and display operational status.

APPLICABLE DOCUMENTS

It is assumed that some of the specifications, standards, and other applicable documents which will govern the design of the power supply defined herein are not presently available. In lieu of these, the following documents shall be used as general guidelines in the design of the power supply. Full compliance with these will likely assure compliance with the final governing specifications when they are issued.

STANDARDS

Military

MIL-STD-202

MIL-STD-461A, Amendment 3 (herein referred to as MIL-STD-461).

MIL-STD-462

MIL-STD-470

MIL-STD-704A

SPECIFICATIONS

Military

MIL-E-5400

DOCUMENTS

MSFC

REQUIREMENTS

General Characteristics

The physical characteristics of the power supply shall be compatible with the overall system packaging concepts, which will be defined at a later date. Special attention shall be directed toward incorporating design features which enhance the on-board maintainability of the supplies. Each replaceable module or subassembly shall be clearly marked with its part number. All replaceable modules or subassemblies bearing identical part numbers shall be physically and functionally interchangeable.

Materials

Materials used in the power supplies defined herein shall be selected in accordance with specifications in the following documents:

Any deviations from the materials specified in the above listed documents shall be brought to the attention of George C. Marshall Space Flight Center for resolution.

Standard Parts

In every case, standard and readily available parts which conform to the requirements of the documents listed above and preferred parts document PPD-600, Volumes 1 and 2, shall be used. In those applications where standard and readily available parts do not exist, a specification control drawing (SCD) for the part

under consideration shall be prepared and submitted to MSFC for approval before incorporation of the part into the design. For the purpose of this specification, standard parts shall be defined as the smallest electronic part of a subassembly which is identifiable as a functional entity; i.e., capacitors, diodes, inductors, integrated circuits, resistors, transistors, etc.

Traceability

The traceability of all parts used in the power supply shall be required and shall be in accordance with Astrionics Laboratory Management Directive AMD 53001.

Metals

Dissimilar metals, as defined in Standard MS33586, shall not be used in combination unless they are suitably coated to prevent electrolytic corrosion.

Nonmetals

Nonmetals shall not support combination or fungus growth and shall conform to the dielectric requirements defined herein.

Functional Characteristics

Fault Isolation/Fail Safe - The power supply defined herein will be powered from a primary voltage source which also powers other critical circuits and power conditioners. The design of the power supply shall be such that no degradation* of the primary power system shall occur when any type of fault or failure occurs in either an LRU connected to a power supply or within the power supply itself. Since the connectors which carry input power to the supply are vulnerable to failures and cannot be protected by fuses or circuits, special attention shall be given to the type of connectors used and their utilization in the supply. In addition, the power supply shall not exhibit any mode of operation, including all possible failure modes, which would result in a hazardous condition to the vehicle or to the crew.

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*Degradation is defined as a condition which causes the operating characteristics of the primary power source to deviate outside the limitations defined in paragraph of this specification.

Fault Detection and Indication - Provisions shall be incorporated into the power supply design to monitor those functions which would indicate that an internal failure has occurred or is likely to occur. If a failure occurs, a signal shall be generated by the supply for delivery to the Data Management System to indicate that the failed supply is non-operational. A failure is defined here as an under-voltage out-of-tolerance of one or more output voltages or a total loss of one or more voltages.

Orderly Start-up and/or Shut-down - Operating voltages must be applied in a prescribed sequence to some of the loads which the power supply will service. Also, if a long-duration primary power drop-out occurs wherein the output voltages of the power supply exceed allowable limits, the operating voltages must be quickly removed from these loads in an orderly sequence. The design of the power supply shall include provisions to apply and/or remove the output voltages from loads in the required sequences.

The shut-down shall be initiated by either of three events:

(a) Receipt of a single electrical command from the Data Management System.

(b) Receipt of a shut-down command from the LRU.

(c) Detection of over-voltage or under-voltage which has occurred after the supply has reached its normal operating voltage.

The orderly shut-down of the power supply shall be completed in a time which will be specified at a later date.

Reliability - The power supply shall provide highly reliable operation when used in any application for which it is designed. The supply shall have a demonstrated mean-time-between-failure (MTBF) of 10,000 hours when operating in the environment defined herein.

Maintainability - The power supply will be used in large, manned space vehicles. Special attention shall be given to incorporating features into the design which will enhance the on-board maintainability of the units, using only those items

of tools and test equipment which are available in the spacecraft. Replaceable subassemblies or modules shall be used to the greatest practicable extent.

Ground test and possibly in-flight tests which will be performed on the power supply probably will utilize automatic test equipment. The design of the power supply shall incorporate those features which will enhance this type of checkout. Among others, features which shall be considered are:

- Sufficient number of test points which indicate the status of various operating elements of the supply. All test points shall be protected against faults to each other and to ground.
- Test connectors which may provide quick access to the unit under test during checkout.

Electromagnetic Compatibility - The power supply shall be electromagnetically compatible with all equipment with which it interfaces. The exact requirements for electromagnetic compatibility for the supply will be defined at a later date. In the interim, MIL-STD-461 and MIL-STD-462 shall be used as guidelines to establish the EMI limitations and test methods for the design of the supply.

Electrical Requirements

A. Input Voltage Range

Steady-State -- 90 Vdc to 125 Vdc

Transient* -- Per MIL-STD-704A

Reverse Polarity -- The power supply shall be capable of withstanding a continuous reversal in the polarity of the input voltage without damage. Recovery to normal operation shall be automatic when normal polarity is reestablished.

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*A new power quality standard is being considered which will replace MIL-STD-704A for future aerospace vehicles. This new document will relax standards on input power quality, particularly for the duration of power interruptions and for the amplitude and duration of spike. It is recommended that MIL-STD-704A be used as a guide until the new standard is released.

B. Source Characteristics

The power supply will be used with a power source which has one of three possible configurations. Figures A-1, A-2, and A-3 show approximate equivalent circuits for these configurations.

C. Ripple Feedback

When operating at full load in any of the power systems discussed above, the power supply shall not cause a ripple current greater than that allowed by MIL-STD-461 to flow in the input lines.

D. Efficiency

The efficiency of the power supply shall be greater than 80 percent for all full-load operating conditions. A design goal for the efficiency shall be 85 percent under the same conditions.

The efficiency of the supply shall be determined by the following relation:

$$E_{ff} = \frac{Pout}{Pin} \times 100\%$$

where:

$$Pout = Pout_1 + Pout_2 + \ldots Pout_n$$

$$= (Eout_1)(Iout_1) + (Eout_2)(Iout_2) + \ldots (Eout_n)(Iout_n)$$

$$Pin = (Ein)(Iin)$$

All voltages are measured at the power supply terminals.

E. Output Characteristics

Output Power - The power supply shall be one design which is capable of supplying between 10 and 150 watts, in the form of one or more output voltages, to multiple loads. The design shall be such that any load power which lies in the above mentioned range can be serviced by one basic design which has modules or circuit cards added (or deleted) as necessary. Provisions shall be incorporated into the design to allow for the parallel operation of outputs which have the same voltage rating. During such parallel operation, the load current shall be shared equally (within 10 percent) by each of the parallel elements. Or

$$i = \frac{I_{load}}{\text{No. of Regulators}} \times 10\%$$

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A	14925	
SCALE	REV.	SHEET

where i is the maximum allowable difference between currents of any regulator. (Note: During parallel operation the combined output power will not exceed a total of 150 watts.)

Output Voltages - The power supply shall have the output voltages shown in Table A-1. Since the outputs may be developed by circuits which have no provisions for precise adjustment, the output voltage may deviate from the nominal value by the tolerances shown in Table A-1. The outputs shall be supplying nominal load current (see Table A-4) when this initial adjustment is made. Other voltages shown in Table A-1 shall be determined at a later date. (Note: No output voltage will exceed ±100 Vdc.).

TABLE A-1. OUTPUT VOLTAGES

Output Number	1	2	3	4	All Others (2)
Output Voltage (V)	+15.0	-15.0	+28.0	+5.0	±4 to ±100
Initial Tolerance (%)	± 0.25	± 0.25	± 0.25	±0.25	± 0.25

Remote Sensing - A means shall be provided on each output of the supply by which the output voltage may be determined at either the load terminal or at the power supply output terminals. If one or both of the conductors which are used to sense the load voltage should fail open, the voltage of that output shall not rise more than 1 percent above the normal, steady-state value. For purposes of circuit design and/or component selection, it may be assumed that the total voltage drop along any pair of power-carrying conductors will not exceed 1.0 volts.

Over-Voltage Protection - Each of the outputs of the power supply shall have a means of detecting an over-voltage condition which might cause damage to sensitive circuits in the loads, and of immediately disabling the failed output. The allowable limits for the amplitude and duration of any output disturbance shall be as shown in Table A-2.

Output Power Levels - The appropriate power allocation for each output voltage of the power supply is shown in Table A-3. The total output power from the supply will not exceed 150 watts.

TABLE A-2. MAXIMUM ALLOWABLE TRANSIENT VOLTAGE AND DURATION FOR OVER-VOLTAGE PROTECTION

OUTPUT VOLTAGE (Vdc)	MAXIMUM VOLTAGE (V)	DURATION (msec)
+15	±5	5
-15	±5	5
+28	±9	5
+5	±1.7	5
Others	±33% of rated output	5

TABLE A-3. TYPICAL POWER ALLOCATIONS FOR EACH OUTPUT - WATTS

Output (V)	+15	-15	+28	+5	All Others (2)
% of Total Power	25	10	35	25	5

Load Transient Response - A step change (0 to 100 percent or 100 to 0 percent) in the load which is connected to any output of the power supply shall not cause a transient (over-voltage or under-voltage) which exceeds the nominal steady-state output voltage by more than the values shown in Table A-2. Any output voltage which is subjected to such a load transient shall recover to the allowed tolerance range (see Table A-5) within the time shown in Table A-2.

Output Currents - The nominal load, minimum load, and full load currents, in amperes, for each output of the power supply are shown in Table A-4.

Voltage Tolerances - The steady-state output voltages of the power supply shall not vary from the nominal value by a deviation greater than the percentage shown in Table A-5. These deviations shall be the total of all error contributions from all possible steady-state sources, including the initial tolerances listed above.

In the following paragraphs, the tolerances specified for line regulation, load regulation, and temperature coefficients of the power supply supply outputs shall be used as design guides.

TABLE A-4. TYPICAL NOMINAL, MINIMUM, AND MAXIMUM LOAD CURRENTS - AMPERES

Output (V)	+15	-15	+28	+5	All Others (2)
Minimum Load	0	0	0	0	TBD
Maximum Load	2.50	1.00	1.80	7.50	TBD
Nominal Load	1.25	0.50	0.90	3.75	TBD

TABLE A-5. MAXIMUM ALLOWABLE ERROR FOR OUTPUT VOLTAGE

Output (V)	+15	-15	+28	+5	All Others (2)
Maximum Error (%)	±2	±2	±2	±2	±2

Line Regulation

When the input voltage is varied over the range of +90 volts to +125 volts, the change in the voltage of any output of the power supply shall not exceed the tolerance shown in Table A-6 for any load current within the limits specified in Table A-4.

TABLE A-6. LINE REGULATION

Voltage (V)	+15	-15	+28	+5	All Others
Output Change-Percent of Nominal	±0.2	±0.2	±0.2	±0.2	±0.2

Load Regulation

When the load current of any output of the power supply changes from the minimum value to the maximum value shown in Table A-4, the output voltage change shall not exceed the tolerances shown in Table A-7. All outputs other than the test output shall be subjected to nominal loading. The Dynamic Load Regulation shall be that which is defined in paragraph .

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TABLE A-7. STATIC LOAD REGULATION

Output (V)	+15	-15	+28	+5	All Others (2)
Voltage Change-Percent of Nominal Value	±1	±1	±1	±1	±1

Temperature Coefficients

The change in any of the output voltages due to a change in the ambient temperature shall not exceed 0.005 percent per degree centigrade over the temperature range of -20°C to +100°C.

Output Ripple Voltage

The ripple and noise voltage present on any of the outputs of the power supply shall not exceed the values shown in Table A-8. The ripple and noise voltages shall include any components due to switching transients caused by preregulators and dc-to-dc converters, including "spikes", and any other noise source except load transients. Measurement of the ripple will be made with a wide-bandwidth (dc to 50 MHz) oscilloscope and high-impedance probe at the output terminals of the power supply. Any component of the ripple which appears on the common line shall be included in the peak-to-peak measurement. This output shall be supplying full load current to a fixed resistive load and the input voltage shall be adjust to +125 volts for this measurement.

TABLE A-8. OUTPUT RIPPLE

Output (V)	+15	-15	+28	+5	All Others (2)
Output Ripple Voltage - Peak-to-Peak (mV)	75	75	150	25	±0.5% of Nominal Output Voltage

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A	14925	
SCALE	REV.	SHEET

Output Impedance

For frequencies from 1 Hz (dc) to 100 Hz, the output impedance of the power supply outputs shall not exceed the values shown in Table A-9. For frequencies from 100 Hz to 100 kHz, these output impedances shall not exceed three times the values shown in Table A-9.

TABLE A-9. OUTPUT IMPEDANCE - OHMS

Output (V)	+15	-15	+28	+5	All Others (2)
Output Impedance Ohms	0.06	0.06	0.6	0.02	(0.04) (Load Res)

Short-Circuit Protection

Each of the outputs of the power supply shall be capable of withstanding a continuous short-circuit or over-current load for any period of time at any specified operating temperature. When any one output is subjected to such a condition, the internal power dissipation of the supply shall not exceed that experienced during normal full-load operation of the supply by more than 10 percent. The values of current at which the outputs shall enter the current-limiting mode will be defined at a later date. If a fault condition exists (short-circuit or over-current) during start-up, the supply will deliver full-rate output current and will produce a fault indication if an under-voltage exists. The supply will recover from such a start-up fault within 1 second after the fault is removed. If the supply had been operating within desired limits and a fault (over-voltage, under-voltage, or short-circuit) occurs or, if, during start up, an over-voltage appears at the output, the supply will automatically shut down. The supply will recover from this condition if the shut-down command is initiated and the start-up command is re-initiated.

Output Commons

The common returns (grounds) for all outputs shall be isolated from each other. All commons shall be isolated from case ground. Each of the commons, including case ground, shall be brought out on a separate pin in the appropriate connector.

Input/Output Isolation

The power supply input common shall be isolated from all output commons by at least 10 megohms.

Duty Cycle for the Power Supply

The power supply shall be required to operate continuously under any combination of input/output conditions specified herein.

Environmental Conditions

The power supply shall provide the performance characteristics defined above when exposed to any combination of the environmental factors listed below.

Temperature - The power supply shall operate as defined herein when exposed to steady-state temperatures which lie in a range between -20°C to +85°C. The power supply shall be capable of withstanding storage temperatures which lie in a range between -55°C and +100°C without incurring damage.

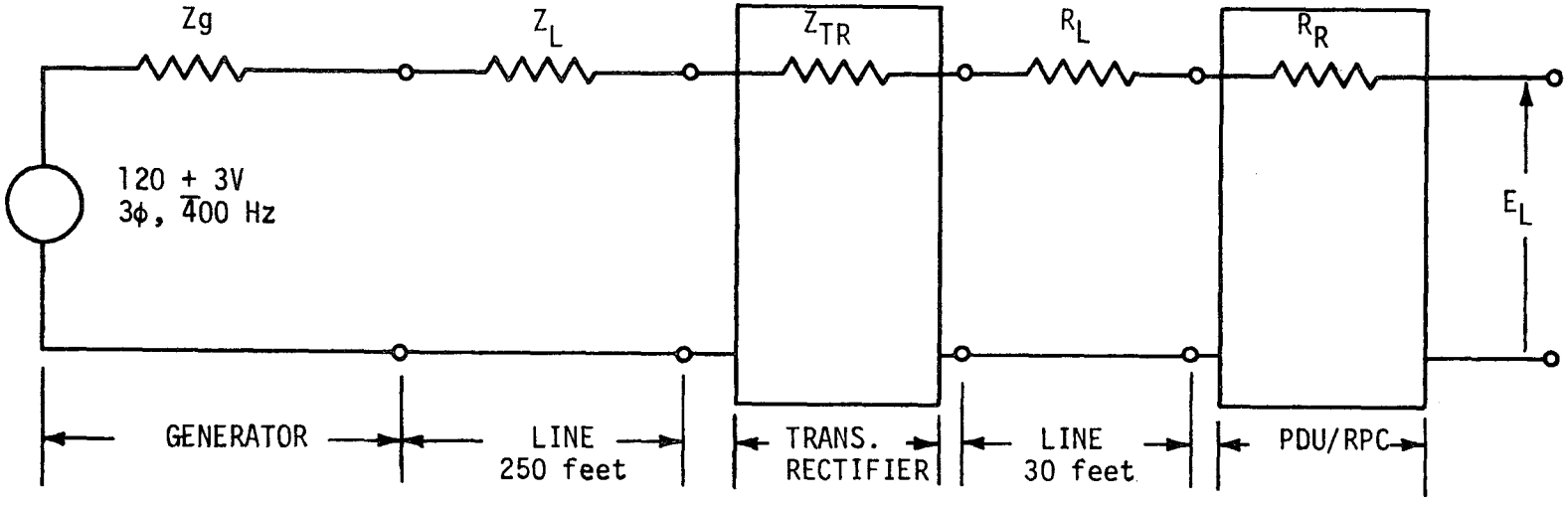
Vibration - The vibration environment for the power supply will be defined at a later date.

Shock - The shock environment for the power supply will be defined at a later date.

Acoustic Noise - The acoustic noise environment for the power supply will be defined at a later date.

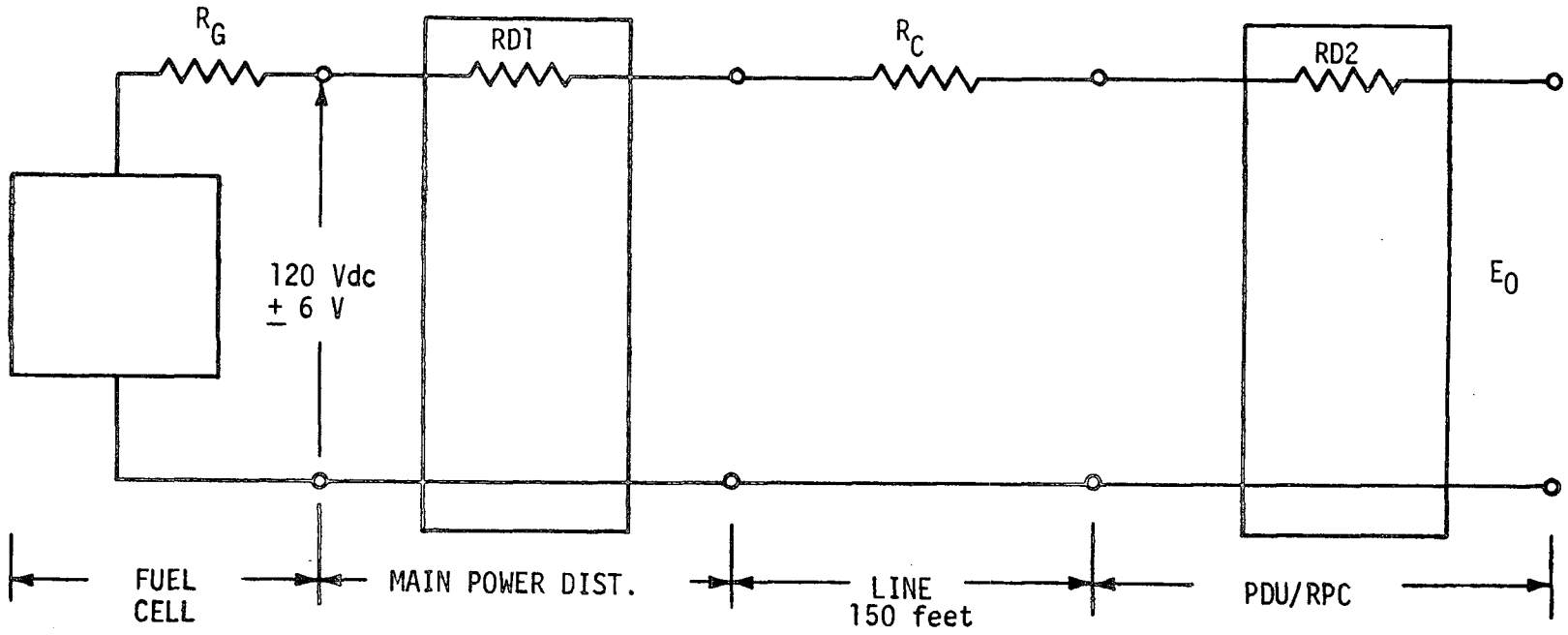
Altitude - The altitude (reduced pressure) environment for the power supply will be defined at a later date.

Salt Atmosphere - The salt atmosphere environment for the power supply will be defined at a later date.



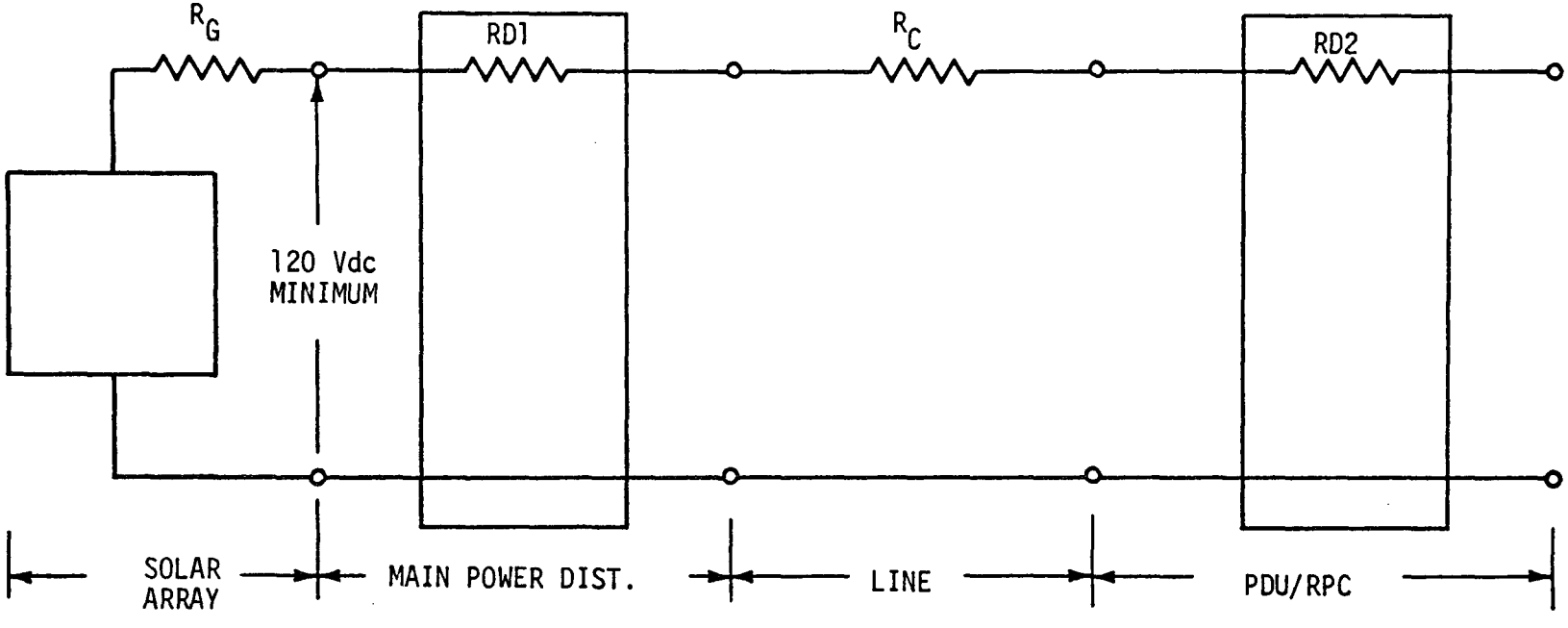
NOTE: IMPEDANCE VALUES TO BE DETERMINED.

FIGURE A-1. EQUIVALENT CIRCUIT FOR BOOSTER EPS



NOTE: PDU/RPC EQUALS POWER DISTRIBUTION UNIT WITH REMOTE POWER CONTROLLER. IMPEDANCE VALUES TO BE DETERMINED.

FIGURE A-2. EQUIVALENT CIRCUIT FOR ORBITER EPS



NOTE: PDU/RPC EQUALS POWER DISTRIBUTION UNIT WITH REMOTE POWER CONTROLLER.
IMPEDANCE VALUES TO BE DETERMINED.

FIGURE A-3. EQUIVALENT CIRCUIT FOR SPACE STATION EPS

APPENDIX B. TRADEOFF STUDY FOR OPTIMUM POWER SUPPLY CONFIGURATION

B.1 INTRODUCTION

A tradeoff study has been performed to establish the best overall configuration for the optimum power supply.* Three candidate configurations have been evaluated to determine the relative cost, size, weight, and electrical performance of each when used in a power system such as that planned for the Space Shuttle. An important note is that, while the primary emphasis was placed on a power supply which would fill the requirements for the Space Shuttle, with minor modifications the conclusions reached in the tradeoff study can be applied to any power system for a large manned aerospace vehicle.

The information used in making this study was derived from the following sources:

- Reports and other documents prepared by the prime contractors for the Space Shuttle
- Experienced gained by Teledyne Brown Engineering during several years of design and development of high-performance airborne power conditioners
- Vendor catalog data and specification sheets
- Data provided by the MSFC Astrionics Laboratory.

B.2 GUIDELINES

Several guidelines for the tradeoff study were established based on the overall requirements for the programs which will utilize the optimum power supply. These guidelines are summarized in the following paragraphs.

*A power supply, or power conditioner, is defined as the black box or module which supplies regulated dc operating voltages to a load.

Primary Source Voltage

A nominal source voltage of 120 Vdc, supplied from rectified 400-hertz ac (Shuttle Booster), fuel cells (Orbiter), or other sources, has been defined for the tradeoff study. Since dc power is the primary source available in the Orbiter, no consideration was given here to using 400-hertz ac for the primary power. For the applications where the conditioned power load is relatively low, 500 watts or less, the use of ac power from inverters may be considered. For higher power loads, it is not deemed practical to use this approach when the primary source of power is direct current.

Load Power Requirements

The magnitude and nature of the loads which the optimum power supply will service have not been completely defined. To establish a workable guideline for sizing the optimum power supply, the study assumed the power levels assigned to the various Line Replaceable Units (LRUs) by MDAC. These power levels are shown in Tables B-1 and B-2.

Equipment Configuration and Placements

The number, location, and power requirements of the various LRUs are shown in Tables B-1 and B-2. The items of equipment are housed in equipment racks or bays which are placed throughout the vehicles.

Redundancy

The overall redundancy requirements (fail operational, fail safe) apply to the power supplies. Further, the failure of an LRU (or

TABLE B-1. LRU POWER REQUIREMENTS AND LOCATIONS IN THE BOOSTER

LOCATION		TOTAL POWER (W)	NUMBER OF LRU
Forward Bay	Left	1799	31
	Right	1769	31
Midship Bay	Left	714	15
	Right	679	15
Crew Stations	Left	351	8
	Center	483	17
	Right	351	8
Aft Top Bay	Left	870	10
	Right	870	10
Aft Lower Bays	Left	522	9
	Right	471	8
Tank Tunnel	Left	30	2
	Right	30	2

TABLE B-2. LRU POWER REQUIREMENTS AND LOCATIONS IN THE ORBITER

LOCATION		TOTAL POWER (W)	NUMBER OF LRU
Nose Bay	Left	90	4
	Right	90	4
Nav. Bay	Left	393	7
	Right	416	8
Forward Bay	Left	1737	19
	Right	1811	19
Wheel Well Bay	Left	210	5
	Right	135	4
Aft Bays	Left	296	13
	Right	296	13
Crew Station Bay	Left	371	8
	Center	503	17
	Right	371	8
	Airlock	60	5

its power supply) must not degrade the performance of any other LRU in any way.

B.3 ASSUMPTIONS

The following paragraphs present the assumptions made to further define the constraints under which the optimum power supply will operate. In general, these assumptions represent typical factors which may be encountered in a large power system. At the same time, they may not be exactly correct for a particular system. However, they do contribute to establishing a baseline for this tradeoff study.

Operating Voltages

The operating voltages required by any particular LRU, and the relative power supplied at those levels, will be as shown in Table B-3.

TABLE B-3. LRU OPERATING VOLTAGES AND POWER LEVELS

VOLTAGE LEVEL (Vdc)	POWER SUPPLIED (% of total per LRU)
+28	35
+15	25
+ 5	25
-15	10
All Others*	5

*It is assumed that two other voltages will be furnished by the power supply.

Equipment Placements

It has been assumed here that the various items of avionics and other loads which use conditioned power will be mounted in groups in one or more locations throughout the respective vehicles. These groups may be considered to be load centers.

B.4 CANDIDATE CONFIGURATIONS

Three basic configurations were evaluated for the optimum power supply. These are

- Central Power Conditioners, wherein four large, centrally located dc-dc power supplies with multiple outputs supply regulated voltages to all LRUs throughout the vehicles.

- Bay Power Conditioners, wherein several (approximately 20) medium power level supplies with multiple outputs are located throughout the vehicles at the load centers (equipment bays). Each supply furnishes regulated voltages to the LRUs located in the same bay.

- Separate Power Conditioners, wherein each LRU has a separate power supply which furnishes it alone with regulated voltages.

Although this tradeoff study considered only these three configurations, they do not represent the only possible arrangements for power supplies in the vehicles under consideration. Combinations of the three basic types of supplies may be more desirable than any one of the three alone for a particular application. However, to keep the scope of this tradeoff study at a reasonable level of effort, the study has been restricted to evaluating only the three basic candidates.

A review of Shuttle documentation showed that a comprehensive tradeoff study already has been performed to evaluate the performance of central power conditioners compared with separate power conditioners using the same basic guidelines and assumptions as those to be used for this study. While a full evaluation of all the parameters covered by this previous study was not possible, in general its conclusions seem reasonable and valid. Thus, to avoid duplicating this effort, the present tradeoff study was restricted to comparing the bay power conditioners with the use of separate power conditioners.

References are made to the use of central power conditioners, or specific data developed in the previous study, when it is pertinent to this present effort. Simplified block diagrams of the configurations which are being evaluated in this study are shown in Figures B-1 and B-2.

B.5 TRADEOFF PARAMETERS

The tradeoff study evaluated the following parameters:

- Cost
- Electrical performance
- Weight
- Size and complexity.

These parameters obviously are not the only factors which will influence the selection of a configuration for the optimum power supply. For example, reliability and maintainability are two very important considerations. However, these factors, and certain others, do not lend themselves to direct comparison between the candidate configurations. This will be discussed in some detail later in this summary.

B.6 DISCUSSION

Cost Considerations

Cost considerations will have significant importance in all future manned spacecraft programs. Therefore, substantial emphasis was placed on determining the cost tradeoff between the candidate configurations for the optimum power supply. Cost data for a number of different types of dc-dc converter regulators have been analyzed to determine the relationship between the magnitude of the output power level and the cost per watt. The results of these analyses are plotted in Figure B-3.

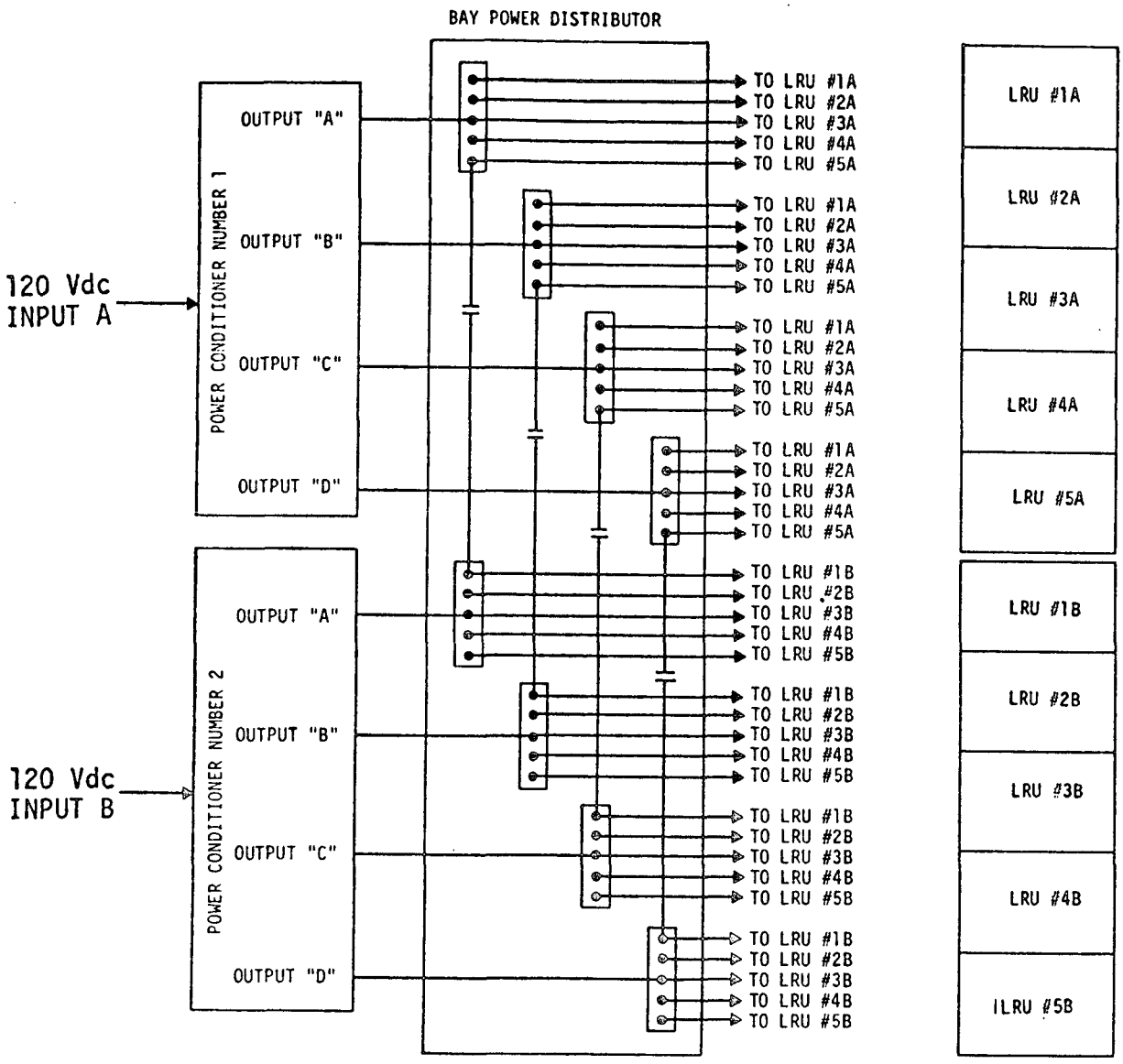


FIGURE B-1. BAY POWER CONDITIONING AND DISTRIBUTION CONCEPT

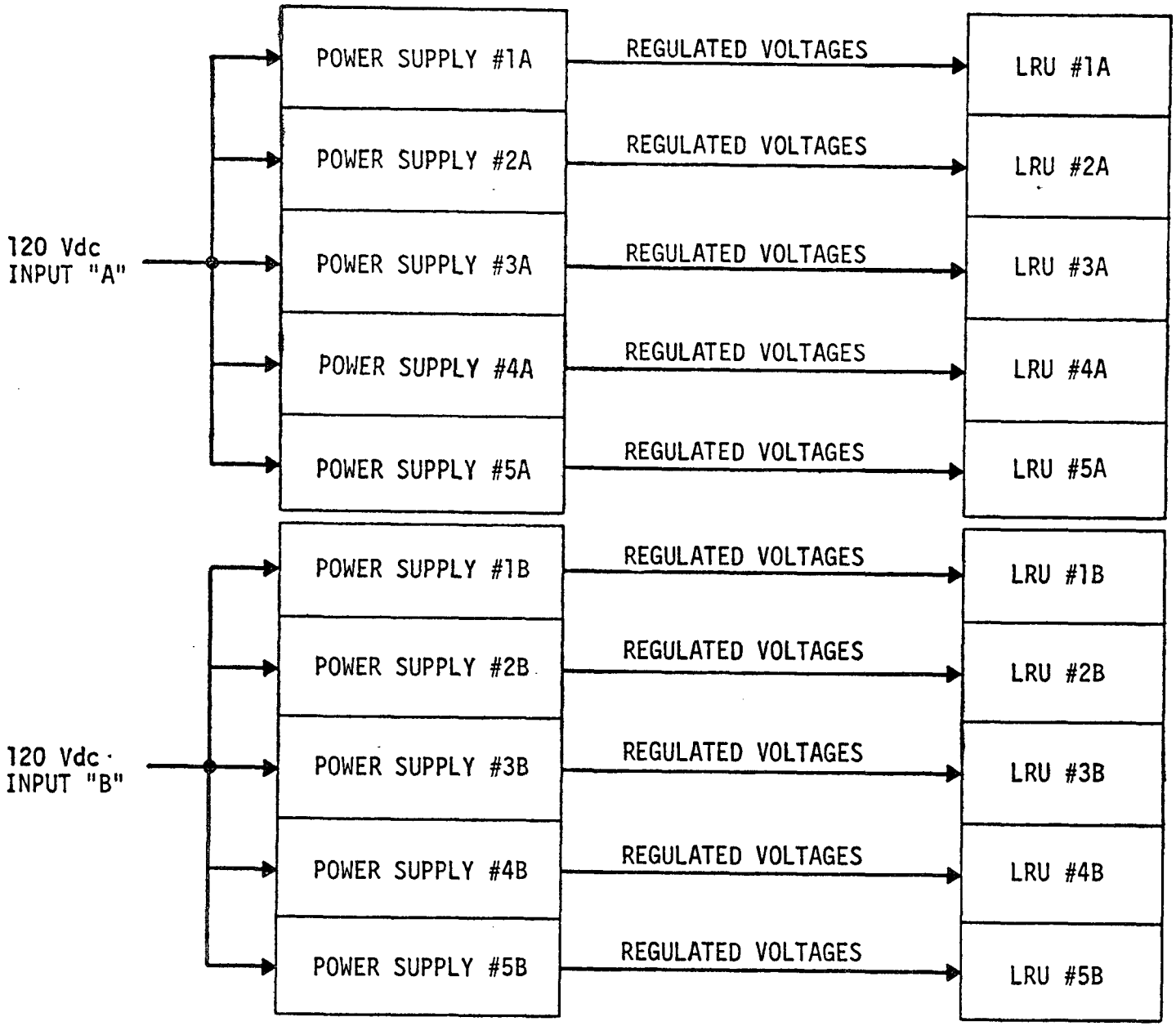


FIGURE B-2. SEPARATE POWER SUPPLY CONCEPT

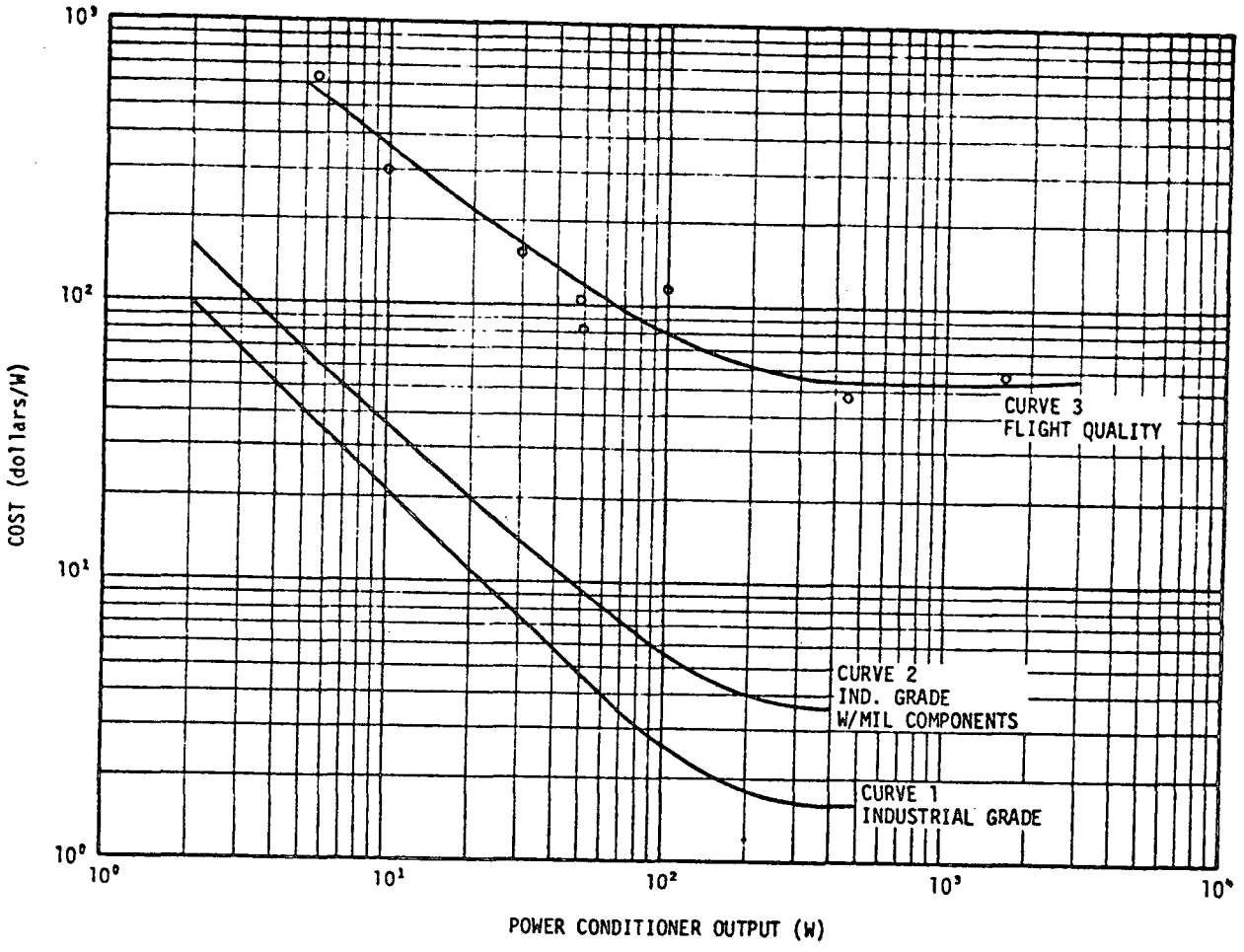


FIGURE B-3. DC/DC POWER CONDITIONER COST PER WATT AS A FUNCTION OF OUTPUT POWER LEVEL

Three curves are shown in Figure B-3. The bottom curve shows the cost per watt of dc-dc type power supplies which utilize industrial grade components and assembly techniques. The middle curve shows the cost per watt for the same type of power supplies except that military grade (JAN) components are used. The upper curve shows the cost per watt for high performance power conditioners and regulators which are intended for use in planned space programs such as ATM. Note that one of the points on the upper curve is the ATM-CBRM. The costs used to derive the curves are recurring; i.e., no attempt has been made to prorate design and development costs into the unit costs for the power supplies. The lower and middle curves were plotted only to show the general trend of the cost per watt for power supplies on which considerable data are available, not to suggest the use of these types of power supplies for future manned space programs.

As can readily be seen in Figure B-3, the cost per watt for all types of power supplies evaluated decreases to a point. For supplies with output power ratings of a few watts to approximately 250 watts, the costs per watt constantly decrease. At 250 watts, the curves assume a relatively constant value.

The data shown indicate that, for a fixed load power requirement, the use of one (or possibly two) relatively large power conditioners will be less costly than using a number of lower power units. As an example, consider the case of a 500-watt load which is evenly distributed among ten LRUs, five active and five identical units serving as redundant backup units. If two 250-watt conditioners are used, with each servicing five of the LRUs, the cost per watt will be approximately $58 per watt (from the upper curve in Figure B-3). The total costs for the two power conditioners would then be:

$$\text{Total Cost} = (250 \text{ watts})(\$58/\text{watt})(2) = \$29,000 \ .$$

Now, if the same load is serviced by ten smaller power conditioners, each of which is rated at 50 watts and powers one LRU, the cost per watt for each supply is approximately $115 per watt. For this case the total cost for the ten power conditioners is:

$$\text{Total Cost} = (50 \text{ watts})(\$115/\text{watt})(10) = \$57,500 .$$

Thus, the use of a relatively small power conditioner for each LRU results in a cost which is approximately twice that of the larger conditioners.

No claim can be made as to the absolute accuracy of these numbers because they have been derived from emperical data. However, it is felt that the overall shapes of the curves shown in Figure B-3 reflect the cost per watt of a power conditioner as a function of its output power, and that the cost per watt is significantly lower for relatively large power conditioners when compared with smaller units. Additional work has been performed to determine if an exact relationship can be derived to express the cost per watt of any power supply (flight quality) as a function of its output power level. Unfortunately, no clear relationship has as yet been derived.

The curves imply that the use of bay power conditioners would result in lower hardware costs than using a separate power conditioner for each LRU. However, in a power system which must fulfill the requirements of the multi-redundant (FO/FO/FS or FO/FS) characteristics of the Space Shuttle, and probably all future large manned spacecraft, it is necessary to provide some means of switching each of the outputs of the power conditioners which service multiple loads. In addition, in this type of application each of the bay power conditioners must be capable of supplying the total load if they are to be fully redundant.

If the switching (or "cross strapping") is performed in an internal assembly, or power distributor, as shown in Figure B-1, the cost of this assembly must be considered in the tradeoff analysis. When these factors are evaluated the cost advantages of the bay conditioners disappear. This may be seen from the following example.

The cost of the power conditioners can be determined using the relationships described previously and data from Figure B-3. From curve 3 in Figure B-3, the cost per watt of a 500-watt conditioner is approximately $55 per watt. The cost for two conditioners for a redundant system then would be:

$$\text{Total Cost} = (500 \text{ watts})(\$55/\text{watt})(2) = \$55,000 .$$

For purposes of this analysis a cost for the power distributor equal to the cost of one of the 250-watt power conditions will be assumed; this appears to be a conservative assumption.

Using these data, the cost tradeoff favors the use of separate power conditioners for each LRU by approximately $12,000. All of the factors are summarized in Table B-4.

An important cost consideration associated with the use of bay power conditioners is the additional time which will be required for extra subsystem design (distribution networks, etc.).

Also, some additional effort will be required for interface definitions, subsystem integration, and coordination. All these factors are somewhat nebulous, but will require time and attention, which means added costs for the bay conditioner approach.

TABLE B-4. SUMMARY OF COSTS OF BAY POWER CONDITIONERS COMPARED WITH SEPARATE POWER CONDITIONERS (500-WATT REDUNDANT LOAD)

COMPONENT	TOTAL COSTS FOR BAY CONDITIONER APPROACH	COSTS FOR SEPARATE SUPPLY APPROACH
a. Two 500-watt power conditioners at $27,500 each	$55,000	-
b. Power distributor at $14,500 each	$14,500	-
c. Ten each 50-watt power conditioners at $5,750 each*	-	$57,500
TOTAL	$69,500	$57,500

*($115/watt) (50 watts) = $5,750

Electrical Performance Considerations

The bay power conditioner configuration has certain inherent features which will result in slightly degraded performance of the overall power conditioning subsystem. These features are the result of transmitting power, in some cases at relatively high current levels, over the networks which interconnect the bay conditioners with the LRU loads. The overall efficiency of the subsystem is reduced because of the losses in the network wiring, and the voltage regulation for load current changes is degraded due to the voltage drops caused by the line resistance. The use of remote sensing for the output voltages of the bay conditioners will provide some compensation for these voltage drops. However, for the LRUs which require large current levels at relatively low voltages it will probably be necessary to utilize a separate voltage regulator in the LRU to provide the necessary degree of regulation.

The design parameters which affect the electrical performance were analyzed to determine the magnitudes of the degradation. To make this determination the equipment bay identified with the largest dimensions is 60 by 45 by 20 inches in the Space Shuttle Orbiter. Using this configuration, the length of the longest power cable was estimated to be 5 feet, or 10 feet of conductors including the ground return. The highest power level for an LRU which would be connected to a bay conditioner was assumed to be 150 watts, which is distributed at four voltage levels, as shown in Table B-5.

TABLE B-5. POWER ALLOCATION FOR OUTPUT VOLTAGES TO 150-WATT LRU LOAD

OUTPUT VOLTAGE (Vdc)	POWER (W)	CURRENT (amps)
+28	52.5	1.8
+15	37.5	2.5
+ 5	37.5	7.5
-15	15.0	1.0

If a conservative wire area of 1,000 circular mils per ampere is used for the conductors which distribute the power, the power lost in the four networks may be determined as follows:

Voltage drop (Vd) across connecting wires

$$Vd = \frac{I \sigma \ell}{A}$$

where

ℓ - length of the conductors

A - cross sectional area of conductors

σ - conductivity of the material (assumed to be copper)

I - current flowing through the wire

for an assumed constant current density; i.e., one thousand circular mils per ampere. For a given wire size, it can be seen that the voltage drop per unit length is:

$$\text{Drop/Unit Length} = \frac{I\sigma}{A} = 0.01 \text{ volt/ft for soft copper.}$$

$$\text{Total Line Drop} = V_d = 0.01 \times 10 = 0.1 \text{ volt}$$

$$\text{Total Power Loss} = P_d = I_1^2 R_1 + I_2^2 R_2 + \ldots I_n^2 R_n \ .$$

Since $I_1 R_1 = I_2 R_2 = \ldots I_n R_n = V_d$

$$P_d = V_d (I_1 + I_2 + \ldots I_n)$$

$$= 0.1 (1.8 + 2.5 + 7.5 + 1.0)$$

$$= 1.28 \text{ watts.}$$

$$\text{Percent loss in subsystem efficiency} = \frac{1.28}{150} \times 100\%$$

$$= 0.8$$

$$\text{Maximum percent loss in line regulation (for 5-volt output)} = 0.1/5 \times 100\% = 2\% \ .$$

Both the power losses and the degraded voltage regulation would be much less severe if a separate power conditioner were to be used for each LRU, since the distance separating the LRU from its conditioner could be made much less than five feet. Ideally, each unit could be placed adjacent to its LRU, thereby eliminating both the power loss and the degraded load voltage regulation incurred in the connecting network.

In addition to the degraded electrical performance discussed above, another problem exists if bay power conditioners are utilized. This problem involves the separation of grounds, or commons, between LRUs located in the same equipment rack which utilize the same voltage levels. While it is possible to provide an isolated ground for each output voltage from a bay power conditioner, it will require a considerably more complex design. This follows because of the highly desirable requirements of having fault detection circuits, orderly start-up/shut-down logic, etc., on each of the isolated outputs.

Weight and Size Consideration

Since unnecessary weight and extra volume in airborne power conditioners result in reduced payload capability for a spacecraft, it is essential that they be minimized where possible. Part of the trade-off study effort described here evaluated the impact on weight and size of the bay power conditioners compared with separate conditioners for each LRU.

An approach similar to that described above under Cost Considerations was used; i.e., data on existing designs were analyzed and the results used to predict the weight and volume characteristics of the two candidate configurations. The results of the analyses are shown in Figures B-4 and B-5. Two curves are shown in each of the figures.

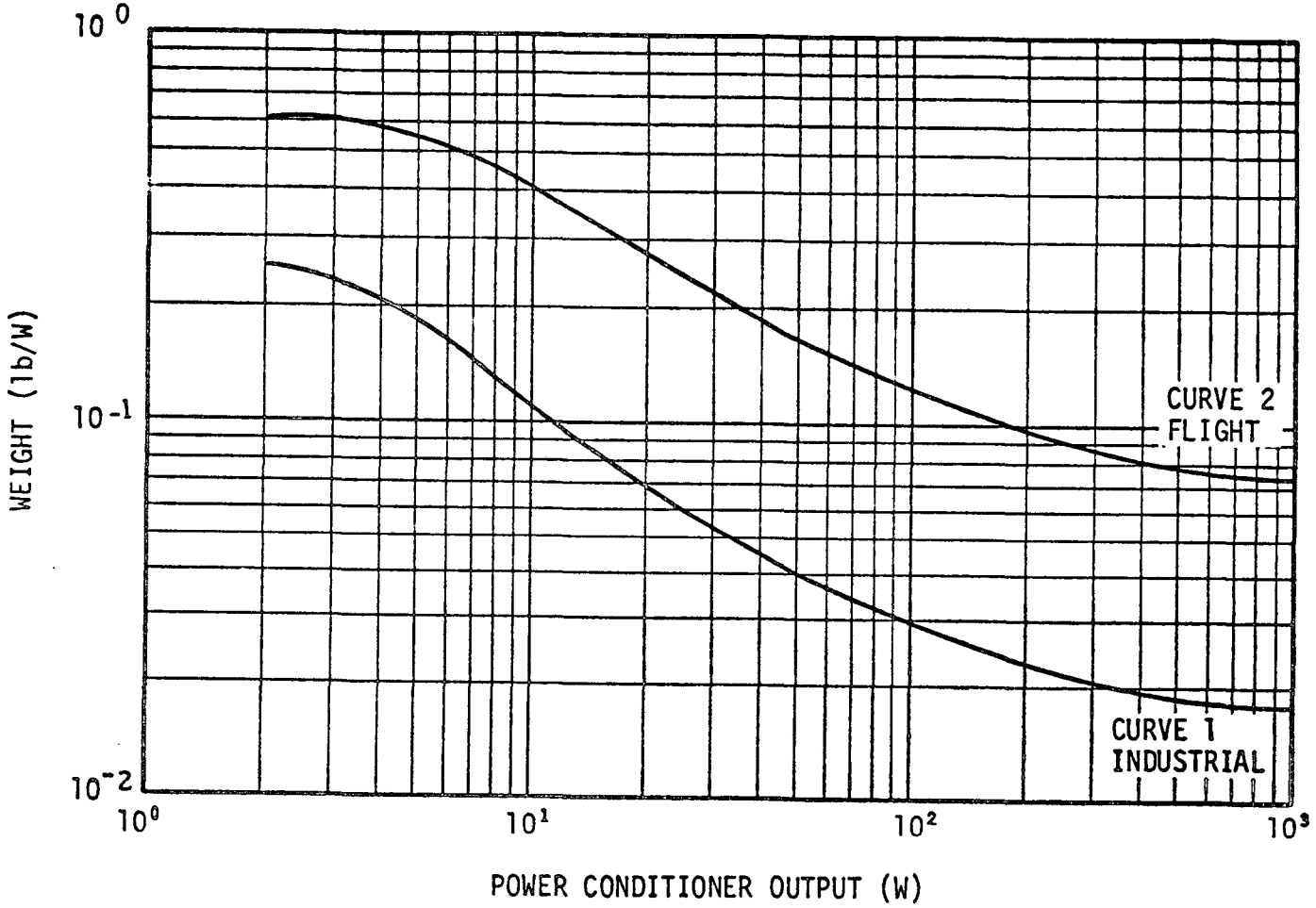


FIGURE B-4. DC-DC POWER CONDITIONER WEIGHT PER WATT AS A FUNCTION OF OUTPUT POWER

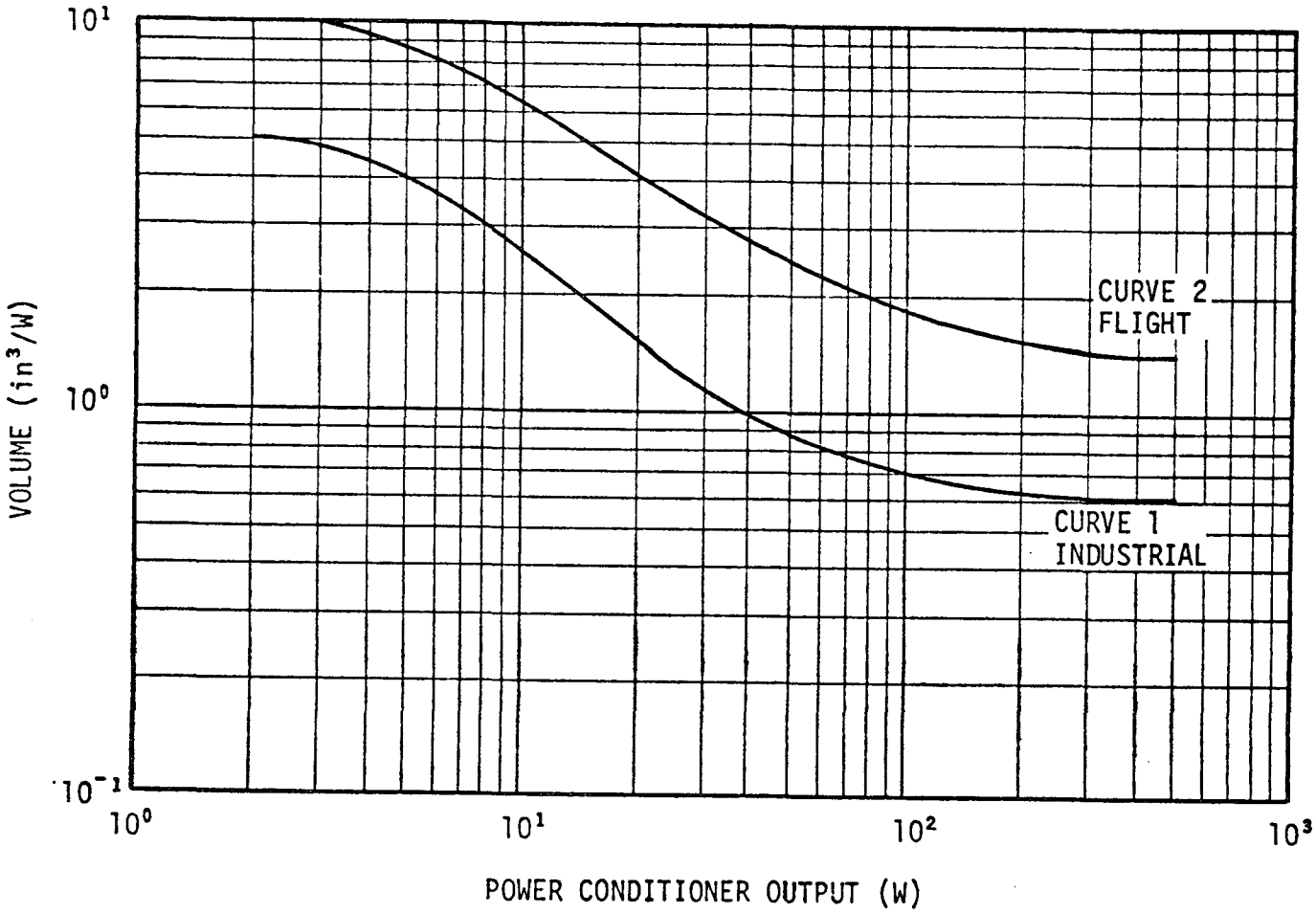


FIGURE B-5. DC-DC POWER CONDITIONER UNIT VOLUME PER WATT AS A FUNCTION OF OUTPUT POWER

The lower curve in both shows the relationship between the output power and the per-watt weight (Figure B-4), or volume (Figure B-5), of dc-dc type power conditioners which are manufactured to industrial standards. The upper curve shows the same relationship for conditioners which will be used in manned spacecraft. Again, the lower curve is shown only to allow comparison of its shape with that of the upper curve.

It is readily apparent from the curves that the weight and volume characteristics of both types of conditioners have the same general shape. This is logical since these factors are closely related. A comparison was made between the weight and volume of the bay conditioners and the separate conditioner for each LRU. The results are tabulated in Tables B-6 and B-7. It is noted that the absolute magnitudes of the weights and the volumes shown in these tables are approximate. However, the results of the comparison are thought to be reliable.

From Tables B-6 and B-7, it may be concluded that the use of bay conditioners will have weight and size advantages only if a nonredundant configuration is used. In a power system which requires the multiredundant characteristics defined for Shuttle, and probably all future large manned spacecraft, these advantages will be offset by the necessity to have a means of bus protection and switching at each output that serves multiple loads. This will add additional weight and extra volume. As a result, the tradeoff favors the use of separate power conditioners for each LRU.

Other Considerations

As mentioned earlier, a number of factors do not lend themselves to a direct comparison in a tradeoff analysis of a bay power conditioner and separate power conditioners for each LRU. Essentially, these factors are:

TABLE B-6. SUMMARY OF WEIGHT OF BAY POWER CONDITIONERS COMPARED WITH SEPARATE POWER CONDITIONERS

COMPONENT	TOTAL WEIGHT FOR BAY CONDITIONER APPROACH (lb)		VOLUME FOR SEPARATE SUPPLY APPROACH (lb)
	REDUNDANT	NONREDUNDANT	
a. Two 500-watt power conditioners	80	45	--
b. Power distributor	20	--	--
c. Ten 50-watt power conditioners, 8.5 lb each	--	--	85
TOTAL	100	45	85

TABLE B-7. SUMMARY OF VOLUME OF BAY POWER CONDITIONERS COMPARED WITH SEPARATE POWER CONDITIONERS

COMPONENT	TOTAL WEIGHT FOR BAY CONDITIONER APPROACH (in^3)		VOLUME FOR SEPARATE SUPPLY APPROACH (in^3)
	REDUNDANT	NONREDUNDANT	
a. Two 500-watt power conditioners	1,400	750	--
b. Power distributor	400	---	--
c. Ten 50-watt power conditioners, 25 in^3 each	--	--	2,500
TOTAL	1,800	750	2,500

- Overall reliability of the power conditioning subsystem
- Fault detection and indication
- Maintainability and repairability.

An accurate comparison of the reliability of a bay power conditioner with either the large central conditioners or separate conditioners for each LRU is difficult because no design now exists for the three types which can be analyzed. However, as a general rule, the reliability will be better for a particular subsystem which has fewer components and connections (especially cable connections) when compared with another subsystem which performs the same function by using more components, assuming that both operate in the same environment. If this rule is applied to the use of either bay power conditioners or separate power conditioners for each LRU, the bay conditioners would be favored since they will have fewer components than the total required for the separate conditioners. If the power distributors which must be used with the bay conditioners are included, then the total number of components and connections for either the bay conditioners or the separate conditioners are likely to be nearly the same. Thus, the reliability of both configurations will be approximately the same.

An additional factor must be considered which is related to the overall reliability of the power conditioning subsystem. If one output voltage of the bay power conditioner should become shorted or otherwise fail, all the connected LRUs must be disabled which use the voltage that has failed, and operation of the redundant units must begin. Referring to Figure B-2, it can be seen that a fault to ground in the power distributor at the location marked by "X" would result in the loss of Voltage "A" to LRUs 1A through 5A. (Of course, a failure of output "A" in Power Conditioner Number 1 could be overcome by opening and/or

closing the appropriate contacts in the distributor and picking up the load on Power Conditioner Number 2.) This deficiency is considered to be a basic shortcoming of the bay power conditioner configuration.

The operations of fault detection and indication would be somewhat simpler in the configuration which utilizes bay power conditioners than in the separate conditioner configuration. A smaller number of comparison circuits and logic functions which monitor the operation of the power conditioner would be required if the bay conditioners are used. Also, less compatibility in the data processing and display subsystems, which will monitor and display overall system status, would be required if bay power conditioners were used. This is based on the number of separate conditioners to be monitored in the two configurations: approximately 160 for the individual conditioner for each LRU and approximately 20 if bay conditioners are used.

At this time the maintainability and repairability of the two tradeoff configurations cannot be analyzed in detail because both of these factors are influenced by the final packaging configuration. Line maintenance, which probably consists of replacing LRUs, should be approximately the same for either configuration.

If the on-board maintenance plan for a flight mission includes replacing modules in the power conditioners, little difference in the effort should be required to maintain either configuration. However, since the number of conditioners involved when each LRU has its own conditioner is substantially higher, more replaceable components must be provided for the separate power conditioners than for bay conditioners. This, in turn, requires extra on-board storage space, etc.

B.7 CONCLUSIONS

The conclusions of this tradeoff study are shown in Table B-8. Almost all the conclusions favor the use of an individual power conditioner for each LRU. Those conclusions which favor bay conditioners do not have overwhelming justification for the use of bay conditioners.

The conclusions of the MDAC tradeoff study which evaluated large central conditioners and separate conditioners for each LRU in the Space Shuttle are restated as follows:

- The weight reduction achieved by using large central power conditioners without cross-strapping between the redundant power buses amounts to only a 20-pound increase in payload capability for the Space Shuttle. If cross-strapping between the four redundant power distribution systems on the booster is used, central power conditioning will result in a 423-pound reduction in payload capability.

- Design development costs are higher for central power conditioning.

- Central power conditioning has a lower reliability

- Power distribution using central conditioning is complicated due to the requirement for seven separate power buses per power system or a total of 28 separate buses in the forward compartments of the orbiter and booster.

- Central power conditioners have a limited growth potential and capability to accommodate system changes.

- Program cost and payload weight impact are shown below:

TABLE B-8. CONCLUSIONS OF TRADEOFF STUDY

TRADEOFF PARAMETER	BAY POWER CONDITIONERS	SEPARATE CONDITIONER/LRU
1. Cost	Cost per watt lower. Additional cost incurred due to need for power distributors and extra system design and integrated efforts.	Cost per watt higher. Overall costs lower since no distributor required. Extra subsystem design and integration cost minimal.
2. Weight and Size	Low weight and size for nonredundant operation. Higher weight and size with cross-strapping.	Size and weight per unit watt higher. Overall weight lower if cross-strapping is used with bay conditions. Weight difference approximately equal to the weight of power distributor.
3. Electrical	Overall power subsystem efficiency lower due to losses in interconnecting networks. Voltage regulation for changes in load current degraded because of line resistances. Use of remote sensing cannot alleviate all of the change. Isolation of grounds between LRUs using some voltages requires extra complexity.	Losses in interconnecting networks minimal or nonexistent due to lack of interconnecting network. Voltage regulation at load essentially equal to that at power conditioner output terminals. Isolation of grounds between LRUs relatively simple as is isolation of commons between different voltage levels in the same LRU.
4. Reliability/ Redundancy	Reliability of conditioners better due to fewer components and connections compared to number of separate conditioners required to serve same load power. Addition to output distributor reduces overall subsystem reliability. Fault of an output voltage in distributor results in shutdown of all LRUs which use that voltage supplied by failed unit.	Failure of output voltage from a power conditioner serving separate LRU results in loss of only that LRU. Other LRUs remain operational.

TABLE B-8 - Concluded

TRADEOFF PARAMETER	BAY POWER CONDITIONERS	SEPARATE CONDITIONER/LRU
5. Fault Detection and Indication	Fewer fault detection circuits required. Data management and display subsystems need less capability to accommodate data on power conditioner status.	Fault detection in circuits required in each power conditioner resulting in increased overall complexity. Data management subsystem must monitor status of each conditioner.
6. Maintainability and Repairability	Line maintenance and on-board maintenance require approximately equivalent level of effort.	Additional repair parts must be provided because of larger number of conditioners.

	PROGRAM COST (in millions of dollars)	PAYLOAD WEIGHT
Central Power Conditioning (without cross-strapping)	61.86	20-lb Increase in Capability
Decentral Power Conditioning	45.95	Baseline

B.8 RECOMMENDATIONS

Based on the conclusions just discussed, it was recommended that the optimum supply be designed such that a separate unit is used to provide operating voltages to each LRU.

APPENDIX C. DESIGN ANALYSES AND TRADEOFF STUDIES

C.1. ANALYSIS OF INVERTER CONFIGURATIONS FOR THE POWER SUPPLY

The purpose of this analysis was to determine the optimum inverter configuration for use in the power supply.

Three basic configurations for the inverters in the power supply were analyzed. These were:

- Single saturated output transformer
- Two transformers in which the input driver transformer saturates
- Two transformers in which neither transformer saturates.

The single transformer approach is the least complicated (Figure C.1-1). The output transformer, since it is permitted to saturate, is of minimum size; therefore, cost, reliability, maintainability, size, and weight would be minimal from a component count standpoint. Briefly, operation of the circuit is described on the following pages.

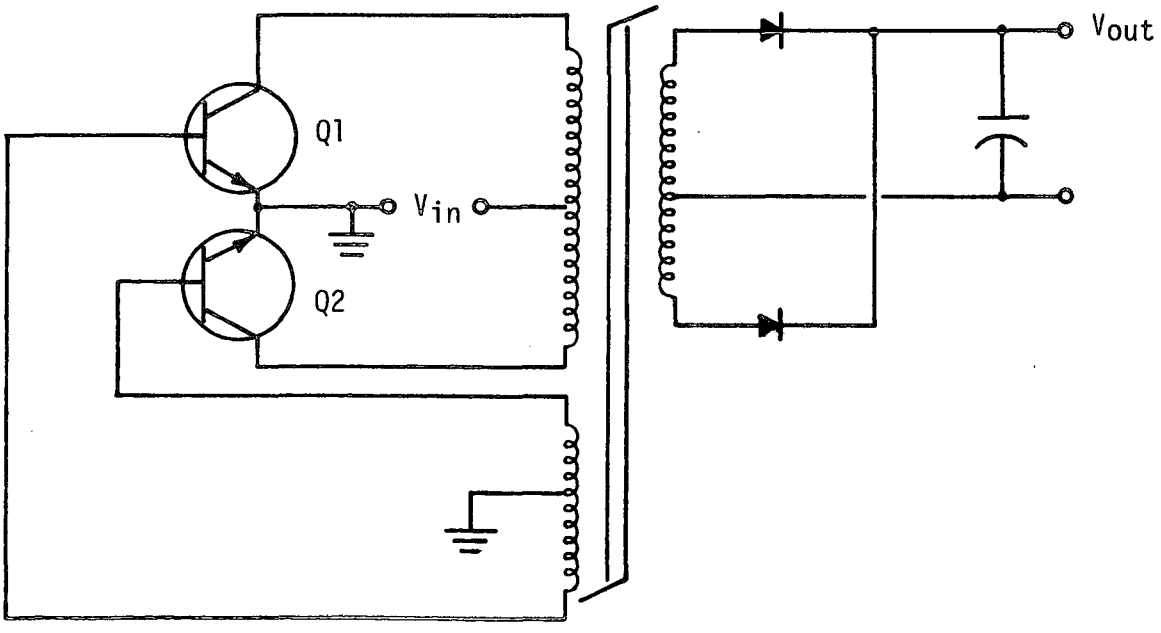


FIGURE C.1-1. SINGLE SATURATED TRANSFORMER DESIGN

When transistor Q1 conducts, the voltage developed across the primary winding of N1 induces a voltage in the feedback windings, N3, which drives Q1 into saturation. Assuming V_{in} is impressed across half the primary winding N1, the flux ϕ must increase in the transformer core at a constant rate $d\phi/dt = V_{in}$. As long as the core remains non-saturated, magnetization current is small, ($i_m \alpha H/N1$), but as saturation is reached, high magnetization current is required to keep $d\phi/dt$ constant. When the reflected load plus the sharply increasing magnetization current exceeds the collector current which Q1 can supply (determined by a base drive and the transistor beta), Q1 begins to pull out of conduction. As the conduction decreases, the collector current decreases, which is regenerative through the feedback winding N3, turning Q1 "off". As flux in the transformer now collapses, a voltage is produced at the feedback winding which begins to turn Q2 on and initiates the next half cycle.

Note that when a transformer is permitted to saturate, high peak currents flow, and switching losses become high as a result of this large current. Also, since switching action occurs during the time high currents are flowing, large switching spikes caused by stored energy in the transformer leakage inductance are impressed on the switching devices and appear at the output. These large switching transients necessitate selection of transistor switches which have higher breakdown voltage and peak current capabilities than would be required if the spikes were not present. These switching transients, since they appear at the input and output, necessitate additional care in the design of the input and output filters.

The converter is self-oscillatory, and its operating frequency is highly dependent on input voltage and output load current.

Part of the problems associated with the single transformer method can be overcome by the use of two transformers. The output transformer is designed not to saturate while a second and smaller transformer, which does saturate, accomplishes the drive function (Figure C.1-2). Because the output transformer is not permitted to saturate, the peak collector current of each transistor is determined principally by the value of the load impedance. This feature provides improved efficiency over the single saturated transformer design.

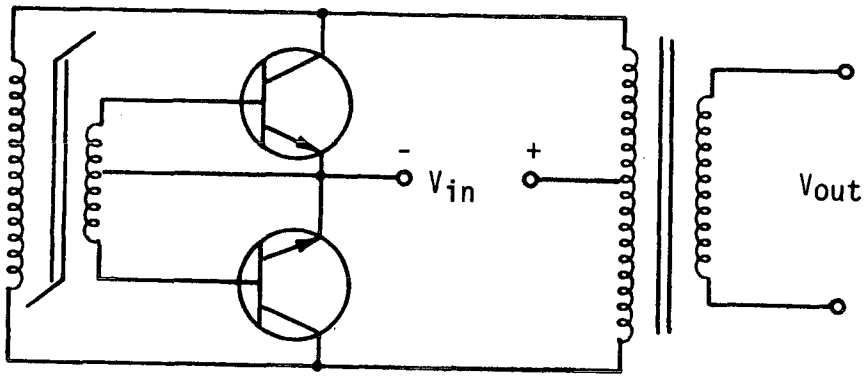


FIGURE C.1-2. TWO-TRANSFORMER CONFIGURATION WITH SATURATED INPUT TRANSFORMER

The magnetizing current can be written as

$$I_M = \frac{H_s M_\ell}{1.26 N}$$

where

H_s - magnetizing field strength at the value of B used

M_ℓ - mean magnetic path length

N - number of turns.

A smaller core is used to perform switching, and a core which has a high permeability can be selected. Using a high permeability, relatively small core enables the value of H_s and M_ℓ to be reduced, greatly reducing the magnetizing current and therefore the losses.

The two transformer inverter configuration in which neither transformer saturates is shown in Figure C. 1-3. This configuration outperforms the previous two configurations. Drive is provided by an external drive circuit such that both transformers are operated in their linear region (non-saturating). Since these transformers are non-saturating, high peak currents associated with saturated transformers are eliminated, increasing efficiency and minimizing component stress. An additional advantage of this configuration is that the operating frequency, which would be determined by an external oscillator, may be externally adjusted and designed to be unaffected by line and load variation. Also since drive is provided by an external low level circuit, control functions, such as remote starting and shut down, can be easily implemented.

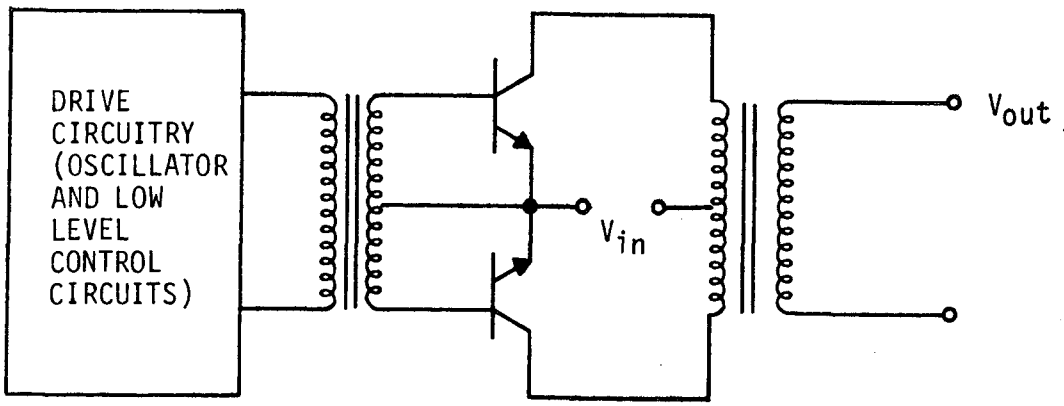


FIGURE C.1-3. TWO-TRANSFORMER CONFIGURATION IN WHICH NEITHER TRANSFORMER SATURATES

This configuration, however, requires additional components in the drive circuit which may degrade the overall reliability and increase the size and weight of this configuration above that of the previous two configurations.

Results of using the two-transformer method are as follows:

- Transistors - switching transistors can be selected that have lower current ratings since the peak currents are substantially reduced. Lower voltage transistors can be selected since they are not required to withstand high energy transients.

- Transformers - Design configuration is more complex because of the addition of a transformer.

- Filters - Filter design requirements are somewhat less stringent since high energy transients are considerably reduced.

In a two-transformer converter package, size would not significantly be increased, cost may be reduced as a result of less stringent requirements on transistors and transformer core, the relatively large output transformer in the single transformer circuit must use expensive square loop materials, and efficiency is greatly improved. The single transformer method cannot be considered optimum. A disadvantage of both configurations is the lack of frequency control and shutdown capability. An optimum configuration would be one in which neither transformer saturates and one in which base drive was proportional to collector current. This would greatly improve the efficiency if it could be accomplished with minimum additional components to maintain optimum cost, size, weight, and reliability.

C.2. A COMPARISON OF SINGLE-ENDED INVERTERS VERSUS PUSH-PULL INVERTERS

The purpose of the analysis presented here is to evaluate two possible configurations for the switching transistors and other elements of a dc-to-ac inverter to be used in the power supply. The two configurations are a "single-ended design and a push-pull design".

C.2.1 PERFORMANCE OF SINGLE-ENDED INVERTERS

The single-ended inverter (Figure C.2-1) operates on the ringing choke principle with no energy transfer taking place during the period in which transistor Q1 conducts. When Q1 conducts, energy is transferred to the primary inductance presented by the primary winding of T1. With Q1 saturated, the voltage V_{in} is placed across the primary inductance, L_p, and the current increases according to $d_i/dt = V_{in}/L_p$ (this assumes that $V_{ce_{sat}}$ is negligibly small compared to V_{in}). Energy, therefore, would be $0.5\ LI^2$ peak. When Q1 is shut off, the energy stored in the primary is coupled to the secondary, through the mutual inductance, and is delivered to the load through diode CR1. The output capacitor, if properly sized, holds the output voltage constant, and the secondary current decreases at a constant rate, $dI_s/dt = V_{out}/L_s$, until some minimum current is reached at which time Q1 is turned on and the cycle repeats.

Since the average input power must equal the output power plus losses, the average input current may be calculated as follows.

By definition

$$\text{Power}_{in} = \frac{\text{Power}_{out}}{\eta}$$

where η is the circuit efficiency, and can be written:

$$\text{Power}_{in} = (I_{\text{primary}_{avg}})\ (V_{in}) = \frac{(I_{out})\ (V_{out})}{\eta}$$

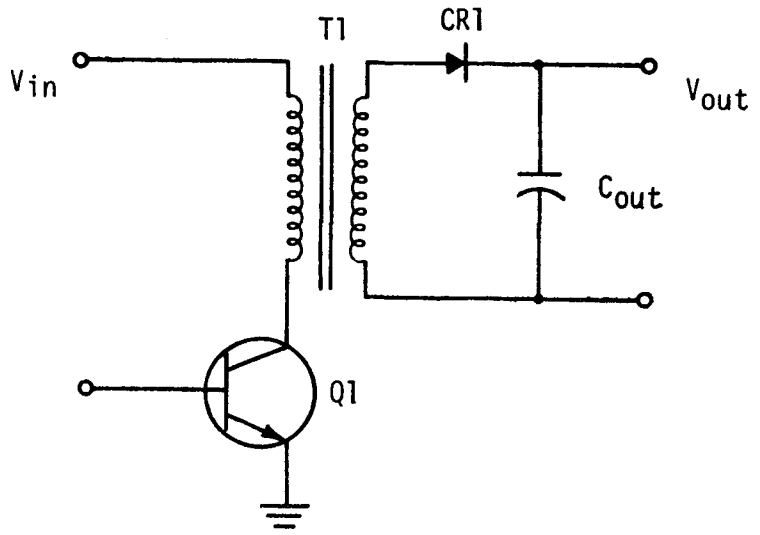


FIGURE C.2-1. BASIC CIRCUIT FOR A SINGLE-ENDED INVERTER

or,

$$I_{primary_{avg}} = \frac{I_{out} \cdot V_{out}}{V_{in} \cdot \eta}$$

Since the current increases linearly in the primary, $d_i/dt = (V_{in})/(L_{primary})$, and taking note that energy is delivered to the load only during the period T_{off}, then

$$d_i = \frac{V_{in}}{L_{primary}} \, dt \quad .$$

The average primary current may be computed as

$$I_{primary}(t) = \int_0^t \frac{V_{in}}{L_{primary}} \, dt = \frac{V_{in}}{L_{primary}} \, t$$

assuming I(0) = 0. Then, the average primary current may be calculated by integrating over the total period (T) as:

$$I_{primary_{avg}} = \frac{1}{T} \int_0^T \frac{V_{in}}{L_{primary}} \, t \, dt$$

$$I_{primary_{avg}} = \frac{1}{T_{on} + T_{off}} \frac{V_{in}}{L_{primary}} \cdot \frac{t^2}{2} \Bigg|_0^{T_{on}}$$

since $I_{primary}(T_{off}) = 0$, and

$$I_{primary_{avg}} = \frac{T_{on}}{T_{on} + T_{off}} \cdot \frac{1}{2} \frac{V_{in}}{L_{primary}} T_{on} \, .$$

Since

$$\frac{V_{in} \cdot T_{on}}{L_{primary}} = I_{primary_{peak}} \, ,$$

then

$$I_{peak} = 2 I_{primary_{avg}} \frac{T_{on} + T_{off}}{T_{on}} \, .$$

Since $T_{on} = T_{off}$, if $V_{out}/V_{in} = N_s/N_p$ at full load, then,

$$I_{primary_{peak}} = 4 I_{primary_{avg}}$$

$$= \frac{4 (I_{out})(V_{out})}{(\eta)(V_{in})} \, .$$

Note also that the flux in the transformer in this configuration is driven in only one direction and not reset, and the maximum permissible flux density swing may be expressed as

$$\Delta\phi = \phi_{max} - \phi_{residual} \quad .$$

Since $\phi_{residual}$ in high permeability materials is quite large ($\approx 0.5\ \phi_{max}$ for supermalloy, $\approx 0.75\ \phi_{max}$ for square permalloy 80, and ≈ 0.25 to $0.50\ \phi_{max}$ for ungapped Manganese Zinc Ferrite materials), gapped ferrite or permalloy powder cores with a low permeability must be used to utilize as much as possible of the ϕ_{max} for the operating flux density swing.

For a given condition of V_{in}, V_{out}, and P_{out}, L_p (primary inductance), $I_{primary_{peak}}$, and N_p (number turns on primary) are fixed, and the primary inductance can be written as

$$L_p = \frac{N_p^2}{I_{primary_{peak}}} \quad (\Delta\phi \times 10^{-8}) \quad .$$

The value of the output capacitor, C_{out}, typically must be such that the time constant, $C_{out}\ R_L$, is at least 10 times larger than T_{on} to assure that the output voltage V_{out} remains essentially constant.

C.2.2 PERFORMANCE OF PUSH-PULL INVERTERS

A description of the operation of the push-pull inverter circuit (Figure C.2-2) follows.

B

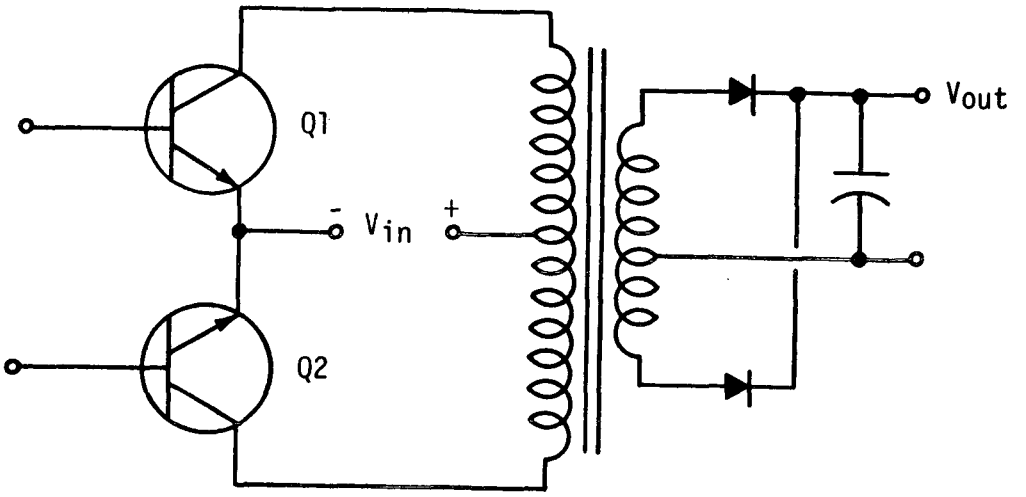


FIGURE C.2-2. BASIC PUSH-PULL INVERTER CIRCUIT

In the push-pull inverter, no use is made of the inductance of the transformer to store energy, as in the single-ended inverter. Instead, energy is transferred to the load continually, except when both transistors are off (which normally is extremely short in duration compared to the period of operation).

At the start of the conduction period for one switching transistor, assume that the flux density in the core is at either its maximum negative value ($-B_{max}$), or its maximum positive value ($+B_{max}$), where B_{max} is the designed maximum flux density and not necessarily equal to B_{sat}. During the conduction of transistor Q1, the flux density changes from its initial level of $-B_{max}$ and becomes positive as energy is simultaneously stored in the inductance of the transformer and supplied to the load. When the flux reaches $+B_{max}$, transistor Q1 is turned off by the driving signal and transistor Q2 is turned on. The transformer supplies energy to the load at a constant rate during the entire period that transistor Q1 conducts. This energy transformation cycle is repeated when transistor Q2 conducts.

Assuming that the full input voltage is impressed across one-half the primary winding, the current flow in the collector of the saturated transistor may be written as

$$\frac{dI_{primary}}{dt} = \frac{V_{in}}{L_{primary}}$$

which can be approximated by

$$\frac{dI_{primary}}{dt} = \frac{2\ I_{primary_{peak}}}{0.5\ T} \quad .$$

Since T_{on} Q1 = T_{on} Q2,

$$\frac{dI_{primary}}{dt} = 4\ I_{primary_{peak}}\ f$$

where f is the frequency of operation, but

$$\frac{dI_{primary}}{dt} = \frac{V_{in}}{L_{primary}} \quad .$$

Thus

$$I_{primary_{peak}} = \frac{V_{in}}{4\ f\ L_p} \quad .$$

The average value of collector current in the conducting transistor is

$$I_{primary_{avg}} = \frac{(V_{out})\ (I_{out})}{(\eta)\ (V_{in})}$$

where η is the efficiency of conversion and the total primary peak current can be written as

$$I_{primay_{max}} = I_{primary_{peak}} + I_{primary_{avg}}$$

$$= \frac{V_{in}}{4\,f\,L_p} + \frac{V_{out}}{\eta\,V_{in}}$$

$$= \frac{V_{in}}{4\,f\,L_p} + I_{out}\,\frac{V_{out}}{\eta\,V_{in}} \quad .$$

Since the transformer is driven in push-pull, the swing on the B-H curve is symmetrical about the origin, and the residual flux density in the core is zero during operation. The maximum permissible magnetic swing is therefore

$$\Delta\phi = \phi_{max} - \phi_{residual} = \phi_{max}$$

where $\phi_{residual} = 0$.

The inductance of the primary can be defined as

$$L_{primary} = \frac{N_{primary}}{I_{primary_{peak}}}\,(\phi_{max} \times 10^{-8}) \quad .$$

In order to provide the same output filtering as provided in the discussion of the single-ended inverter, the output capacitor time constant, $C_{out}\,R_L$, should be 10 times larger than T minus ($T_{on}Q1 + T_{on}Q2$), the period which both transistors are off. A comparison of the peak currents in the single ended inverted [$I_{primary_{peak}} = 4\,I_{out}(V_{out}/\eta \cdot V_{in})$]

and the push-pull inverter [$I_{primary_{max}} = V_{in}/4 \cdot f \cdot L_p + I_{out}(V_{out}/\eta \cdot V_{in})$]* shows that currents in the single-ended circuit are four times greater than the push-pull circuit inverter is greater than the single-ended inverter for similar cores.

C.2.3 CONCLUSIONS

Push-Pull Inverter

Transistor Requirement - Lower peak currents enable selection of lower cost and, in general, higher speed transistors. Also, since the peak currents are lower, higher beta and lower saturation voltage transistors can be used as switches. This will provide higher circuit efficiency.

Transformer Requirements - Since the usable flux density, $\Delta\phi$, in a push-pull design is 25 to 50 percent greater for a given core, and because the primary inductance is not required to store energy, higher permeability, ungapped, and smaller cores may be used. The ability to utilize higher permeability cores enables the transformer to be more efficient. Higher currents and larger leakage inductance of the single-ended design cause high-energy transients to be impressed across the drive transistor and coupled to the output, complicating filter design and transistor requirements.

Filter Requirements - The single-ended inverter design only supplies energy to the load typically one-half the time. Under full-load conditions, the output filter requirements become quite stringent. Ripple currents flowing in the capacitors are high, necessitating the use of larger and, in general, more costly capacitors. In addition,

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*Note in the push-pull inverter, $V_{in}/4\ f\ L_p$ can be minimized by adjusting f and L_p such that $V_{in}/4 \cdot f \cdot L_p << I_{out}\ (V_{out}/\eta \cdot V_{in})$.

losses resulting from the higher ripple currents in the filters become significant.

C.2.4 SUMMARY

At first glance, the cost and size of the single-ended inverter design may seem to be significantly less than the push-pull configuration. However, this is not true. Larger transformers, more complex filters, and higher performance transistors required by the single-ended design cause cost, size, and weight to become high.

Efficiency is also poor in the single-ended design. Therefore, it may be concluded that a push-pull inverter design has advantages in size, cost, and performance, thus eliminating the single-ended configuration from further consideration.

C.3. ANALYSIS OF CANDIDATE OUTPUT VOLTAGE REGULATORS

The purpose of the analysis presented here was to select the optimum type of output voltage regulator which would be suitable for use in arrangement three of the power supply design.

Six basic types of voltage regulators were analyzed for use as output regulators. These were:

- Series linear regulator
- Shunt linear regulator
- Ferroresonant transformer
- Magnetic amplifier (saturating reactor) regulator
- Series switching regulator
- Shunt switching regulator.

C.3.1 LINEAR REGULATORS (SERIES AND SHUNT)

Linear regulators are composed of two basic types: series pass and shunt. As illustrated in Figures C.3-1 and C.3-2, the basic components of each type of regulator are essentially the same.

In the series regulator, a sample of the output voltage is compared with a reference voltage. Any difference between these voltages causes the voltage drop across the regulating element to be varied such that the output voltage is maintained constant.

In the shunt regulator, the regulating element is in parallel with the load and regulates the output voltage by shunting more or less current through the regulator, thereby maintaining a voltage drop across the series resistor such that the output voltage remains constant.

Neither type of regulator provides an advantage with respect to cost, maintainability, flexibility, weight, and size since both regulators are composed of the same basic elements. However, some major circuit performance differences exist.

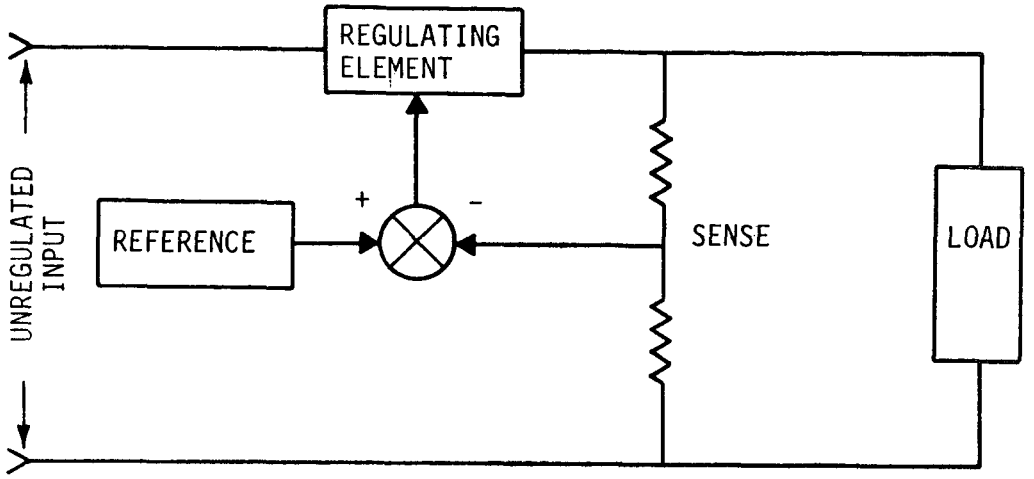

FIGURE C.3-1. SERIES REGULATOR

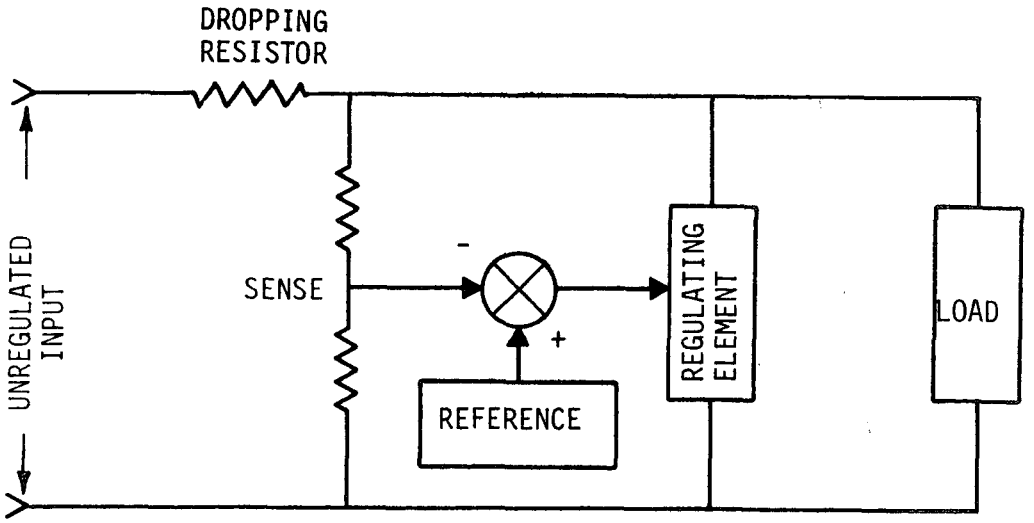

FIGURE C.3-2. SHUNT REGULATOR

Shunt regulators are capable of regulating when the load supplies power, as with inductive loads. Current changes in the load are not likely to reflect back into the raw dc since the regulating element is a current sink. However, the major and most prohibitive disadvantage of the shunt regulator, which eliminates it from further consideration, is its extreme inefficiency. For a fixed input voltage, the power consumed by the regulator plus load is fixed exclusive of the power delivered to the load. Therefore, the maximum efficiency attainable at one-half load is 50 percent.

Series regulators exhibit improved efficiency over shunt regulators. However, if the input-to-output voltage differential becomes high, as it would be during high input line conditions, efficiency decreases. The maximum attainable efficiency with the series regulator may be expressed as a function of the input-to-output voltage, or:

$$\text{Percent Efficiency} = \text{Output voltage/Input voltage} \times (100\%).$$

C.3.2 FERRORESONANT TRANSFORMERS

A ferroresonant transformer consists of a separate primary and secondary winding coupled by a magnetic structure, as shown in Figure C.3-3. A magnetic shunt separates these windings, and the secondary winding is made resonant at the line frequency. When excited by the line source, the resonant circuit builds up enough flux to saturate the core of the transformer on each alternate half cycle. The energy is interchanged back and forth between the magnetic field and the electrostatic field of the capacitor. With the operating frequency fixed by the excitation frequency, the voltage of the capacitor can be expressed in terms of that frequency, or

$$C_{\text{capacitor}} = 4 N \phi_s f$$

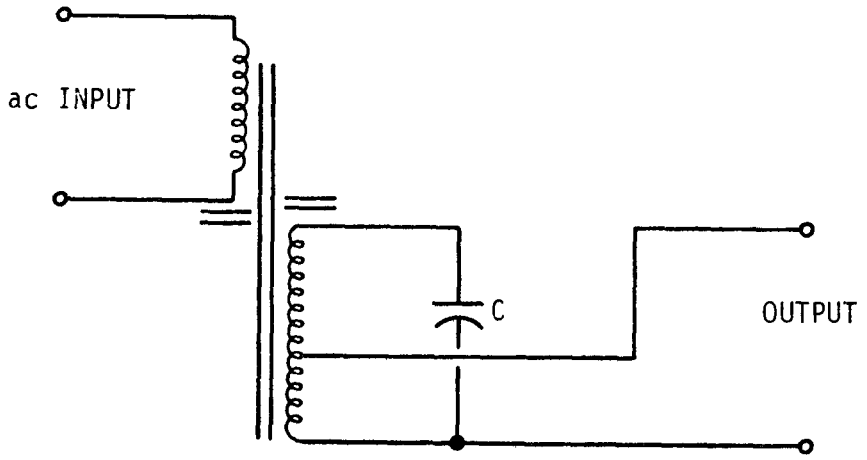

FIGURE C.3-3. FERRORESONANT TRANSFORMER

where

N - number of turns

f - operating frequency

ϕ_s - saturated flux density.

For a constant frequency, the voltage of the capacitor is constant and essentially independent of the input amplitude. This method of regulation gives fairly good line regulation, on the order of ±1 percent, with a minimum of circuit complexity, a high degree of reliability, moderately high efficiency, and low cost. However, this method utilizes relatively large components and has poor load regulation qualities, on the order of ±5 percent. For these reasons it was dropped from further consideration.

C.3.3 MAGNETIC AMPLIFIERS

A basic magnetic amplifier regulator consists of two transformers, each consisting of a primary and secondary winding wired as shown in Figure C.3-4.

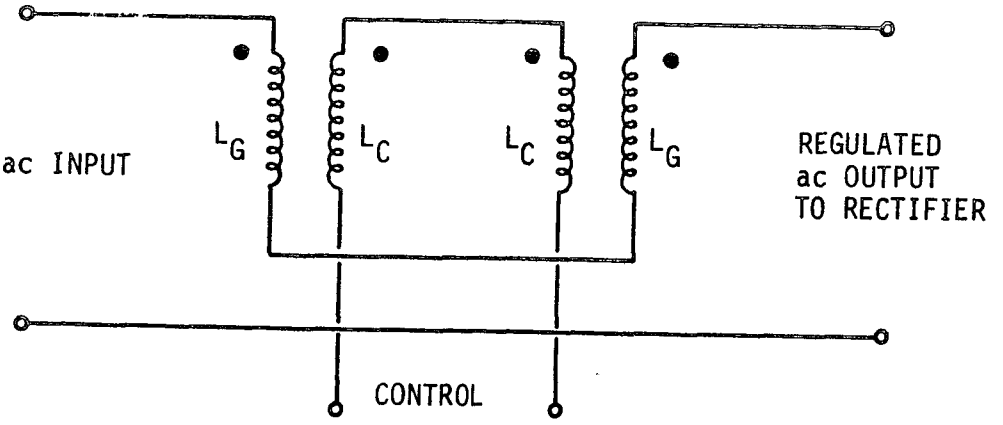

FIGURE C.3-4. MAGNETIC AMPLIFIER

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The power of gate winding, L_G, is supplied by an ac power source in series with the load. A direct current from a control source flows through the control winding, L_C, and partially saturates the core, thereby determining the operating point on the magnetization curve. Hence, a displacement of the operating point results in saturation of the core as soon as the volt-time integral per turn reaches the value equal to the difference between the saturation flux density of the core and the flux density set up by the control winding. When the core saturates, the source current is limited only by the load, and the full source voltage appears across it. By adjusting the control current, the length of time which the core saturates each half cycle can be altered and pulse-width-modulated regulation results.

Magnetic amplifiers can be designed to have high power gains and to be extremely efficient, with typical levels of efficiency exceeding 90 percent at reasonable output current levels. However, some major drawbacks are associated with this approach.

First, at zero control current the inductance of the gate winding must be large to block current from flowing to the load. Since a large inductance necessitates a large number of turns on the gate winding, and since the core must not saturate, relatively large cores must be used.

Second, since the number of ampere-turns on the gate winding equals the ampere-turns on the control winding and the power gain is directly proportional to the ratio of these windings, the inductance and, therefore, the number of turns on the control windings are large.

Third, the response of a magnetic amplifier is proportional to the power gain and can be expressed as

$$T_c = \frac{1}{2f}\left(\frac{R_o}{R_c}\right)\frac{N_c^2}{2N_G^2} \quad \text{seconds}$$

where

f - operating frequency

R_o - load resistance

R_c - control winding resistance

N_c - number of turns on the control winding

N_G - number of turns on the gate winding .

As can be seen from this equation, if high power gains are achieved to maintain high efficiency, an extremely long response time to transients results.

Although the magnetic amplifiers are efficient, they are comparatively large and offer poor response to line and load variations. These reasons were the basis of rejecting the magnetic amplifiers from further consideration.

C.3.4 SWITCHING REGULATORS

As shown in Figures C.3-5 and C.3-6, switching regulators are composed of two basic types: series switched and shunt switched. The shunt switching regulator has the advantage of producing a higher output voltage than the input voltage. However, the peak currents in this regulator for a given input voltage are higher than for the series type regulator since energy is not continually delivered to the load. This, along with the fact that the energy must be stored in the inductor before it can be delivered to the load, makes the shunt regulator somewhat less efficient than the series regulator. Since no requirement exists for a higher output than input voltage, only the series-type switching regulator will be analyzed.

Basically, the series switching regulator operates in the following manner. When transistor Q1 is turned on, current is supplied to

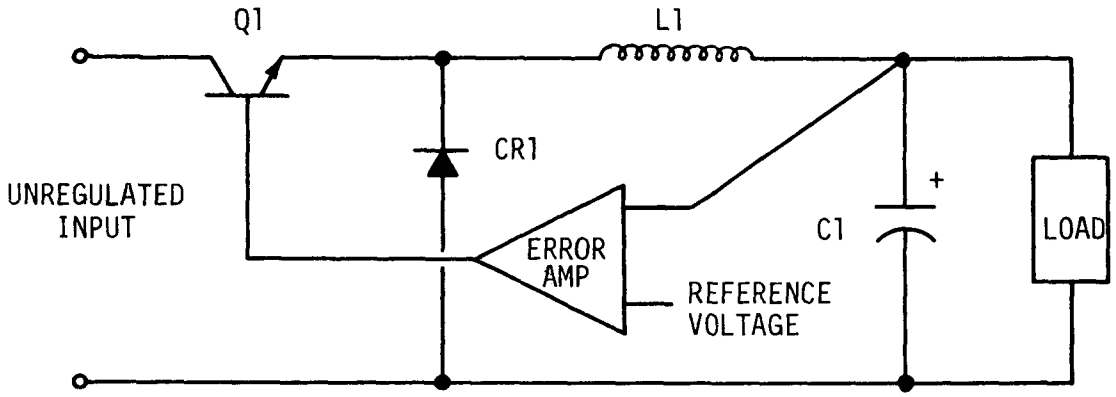

FIGURE C.3-5. SERIES SWITCHING REGULATOR

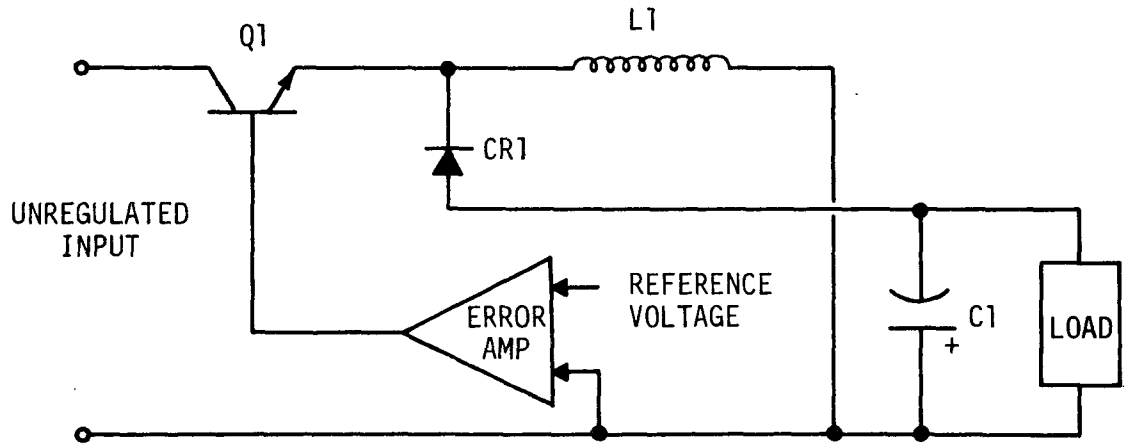

FIGURE C.3-6. SHUNT (BOOST) SWITCHING REGULATOR

the load and, simultaneously, energy is stored in the inductor (L1) and capacitor (C1). While Q1 is off, current is supplied to the load by the capacitor and through CR1 by the inductor. The on and off time of the switch (Q1) is adjusted such that the output voltage remains constant over line and load variations.

The major contributors to power loss in this regulator are the switching transistor and commutating diode, CR1. Since these losses are moderate, high efficiencies can be attained, on the order of 95 percent, without sacrificing performance as in the magnetic amplifier regulator.

C.3.5 SUMMARY

Although linear regulators offer some size, weight, and cost advantages over the other types of regulators, they are relatively inefficient. This inefficiency, when considered with requirements imposed by thermal conditions, complicates packaging.

Ferroresonant transformer regulators have some advantage with respect to complexity and reliability; however, they offer poor and unacceptable load regulation qualities. These regulators also are relatively large.

Magnetic amplifiers offer high efficiency and, generally, a high degree of reliability. However, they also are somewhat large and have comparatively low bandwidths, which makes them a poor choice when considering response to transient line and load variations.

Switching regulators are highly efficient and can be packaged in a relatively small volume if a suitable operating frequency is selected.

These regulators are not extremely complex and are relatively reliable, although the magnetic amplifier regulator offers a greater reliability with less complexity. However, the circuit performance of a switching regulator is enhanced since higher bandwidths are attainable.

C.3.6 CONCLUSIONS

Although a tradeoff must be made between complexity and reliability, the switching regulator was chosen as the optimum candidate for the output regulator in arrangement 3. The choice was based mainly on the high performance capability, high efficiency, and comparatively small size of the switching regulator.

C.4. ANALYSIS OF TRANSFORMER POWER LOSSES

The purpose of this discussion was to optimize a given transformer design.

Core loss in a transformer may be approximated by*

$$P_{core} = a f^2 B_m^n + b f B_m^2 + cf \qquad (1)$$

where

a, b, c - constants which are dependent on the type of core material

f - frequency, hertz

B_m - flux density, gauss

n - constant, depending on the type of core material.

Copper losses are expressed by

$$P_{cu} = \left(I_{RMS}^2\right)\left(R_{DC}\right) \qquad (2)$$

where

$$R_{DC} = \rho \frac{\ell N}{A_{wire}}$$

ρ - resistivity of copper, ohm-in^2

ℓ - length per turn

N - number of turns

A_{wire} - cross sectional area of wire in square inches

I_{RMS} - the rms value of the transformer current.

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*This equation is empirical and is not exact since the constants change with frequency and flux density.

Given a core having a window area W_a and a mean length per turn, ℓ, the following equation can be written:

$$(N)\ (A_{wire}) = (\text{form factor})\ (W_a)\ (\text{fraction of core to be utilized}) \ .$$

The form factor, which is the packing factor of the windings, is 0.5 for most cores. The fraction of the core window area to be utilized for one primary winding is 0.25 since operation is push-pull (two primary windings) and assuming that one-half the core window area is used for the primary winding. Therefore,

$$(N)\ (A_{wire}) = (0.5)\ (W_a)(0.25)$$

$$(N)\ (A_{wire}) = 0.125\ W_a \qquad (3)$$

$$A_{wire} = \frac{0.125\ W_a}{N} \ .$$

Now, by substituting in Equation 2, the equation for wire resistance can be rewritten as

$$R_{DC} = \rho \frac{\ell\ N}{\left(\frac{0.125\ W_a}{N}\right)} = \frac{\rho\ \ell\ N^2}{0.125\ W_a} \ .$$

Assuming that power losses in the primary winding due to copper will be equal to the copper losses in the secondary winding, which will be true if half the window area is utilized for the secondary, then:

$$P_{cu} = (2)\ (I_{in_{rms}})^2 \left(\frac{\rho\ \ell\ N^2}{0.125\ W_a}\right)$$

where $I_{in_{rms}}$ is the transformer primary rms current. Since $\rho = (716)(10^{-9}$ ohm-in$^2)$, for annealed copper, then

$$P_{cu} = \left(\frac{2}{0.125}\right)(716)(10^{-9} \text{ ohm-in})\,(I_{in_{rms}})^2\left(\frac{\ell\, N^2}{W_a}\right)$$

$$P_{cu} = (11500)(10^{-9} \text{ ohm-in})\,(I_{in_{rms}})^2\left(\frac{\ell\, N^2}{W_a}\right) \quad . \tag{4}$$

Now, the specified nominal input voltage for the standard power supply is 115 Vdc, and assuming a maximum power output (one regulator) of 52.5 watts at 85 percent efficiency, then

$$I_{in} = \frac{(52.5) \text{ watts}\left(\frac{1}{0.85}\right)}{115 \text{ Vdc}} = 0.540 \text{ amps} \quad .$$

Therefore

$$P_{cu} = (11500)(10^{-9})\,(0.292) \text{ amp}^2 \text{ ohm-in}\left(\frac{\ell\, N}{W_a}\right)$$

$$= (3350)\,(10^{-9} \text{ amp}^2\text{-ohm-in})\left(\frac{\ell\, N^2}{W_a}\right) \quad . \tag{5}$$

Since Equation 1 for core loss is not exact, data for several cores and core materials were plotted (losses as a function of number of turns) to determine total transformer losses.

The total transformer losses ($P_{transformer}$) are found by

$$P_{transformer} = \text{Core Loss (at } B_m) + 3350 \text{ amp}^2 \text{ ohm-in}\left(\frac{\ell\, N^2}{W_a}\right)$$

where

$$B_m = \frac{(E)(10^8)}{4NfA_c} \qquad \text{(Maxwell's equation for square wave drive)}$$

$$B_m = \frac{(115)(10^8)}{4NfA_c} \tag{6}$$

and

A_c - effective cross sectional area of the core

f - operating frequency, hertz

N - number of turns

E - operating voltage (115 Vdc)

B_m - operating flux density.

Figures C.4-1 through C.4-4 present curves representing the total transformer losses of various transformers utilizing different core materials. The data shown in Figure C.4-1 represent losses for various cores, all of which have the same overall finished physical size, plotted for three frequencies as a function of the number of primary turns. Figures C.4-2, C.4-3, and C.4-4 represent ferrite toroids of increasing physical size for three frequencies as a function of the number of primary turns.

The curves were plotted on the basis of total losses:

$$P_{\text{total loss}} = \text{Core Loss} + \text{Copper Loss} \quad .$$

Core losses were obtained by computing the operating flux density, Equation 6, given the number of turns, core parameters, and frequency and reading of the core losses from a chart for that specific

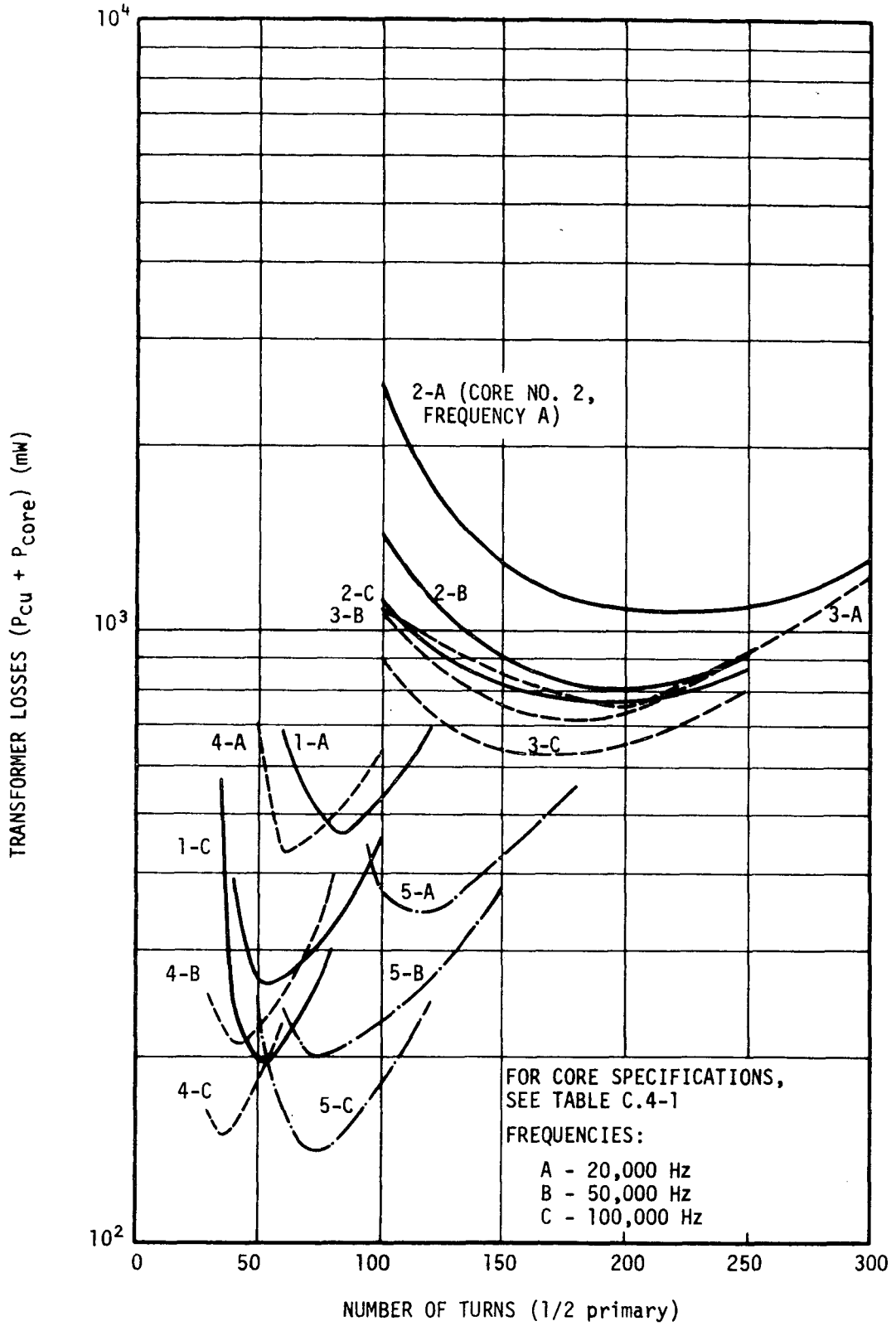

FIGURE C.4-1. LOSS CHARACTERISTICS OF VARIOUS CORE MATERIALS

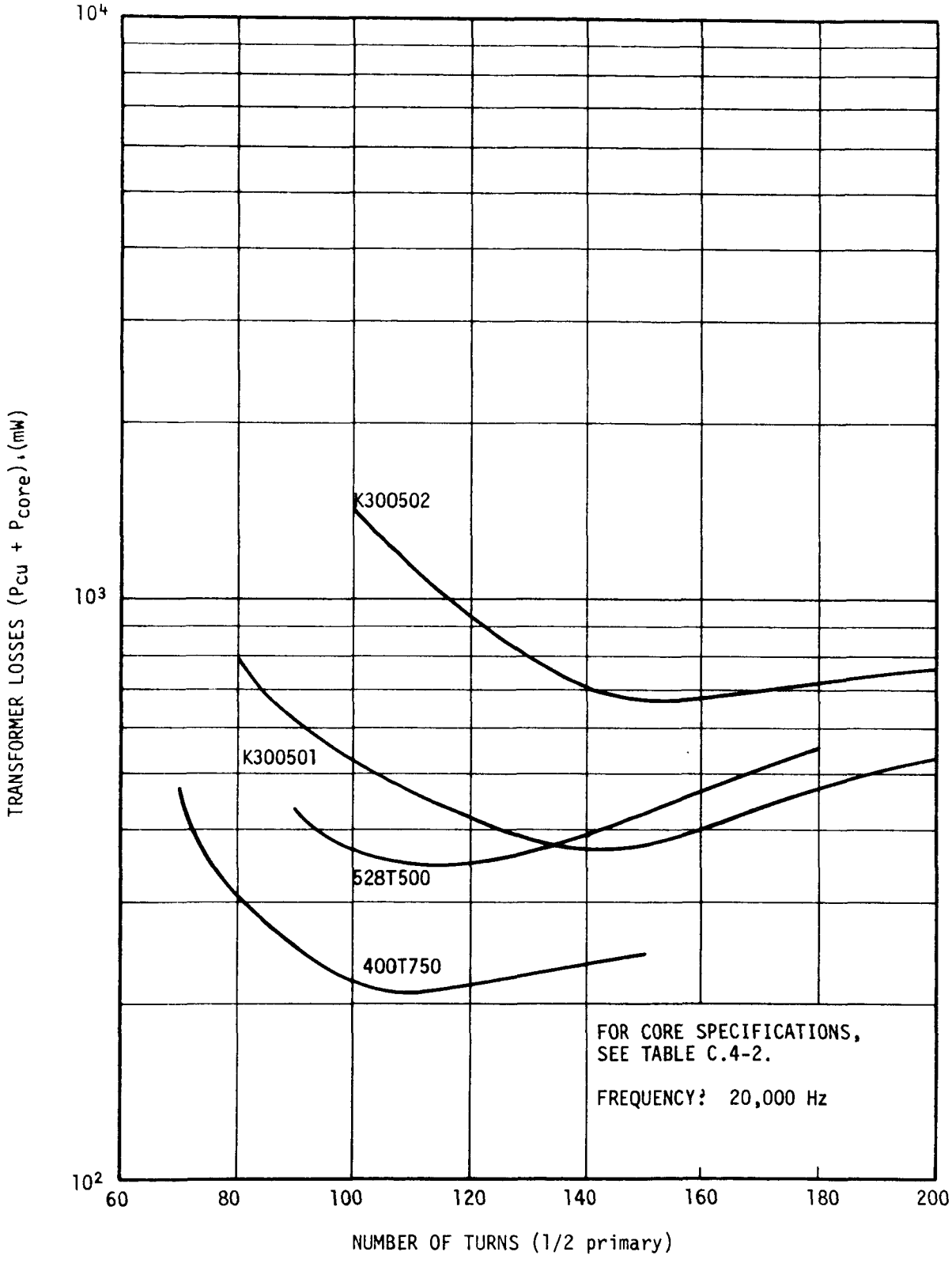

FIGURE C.4-2. LOSS CHARACTERISTICS OF VARIOUS FERRITE CORE SIZES AT 20,000 HERTZ

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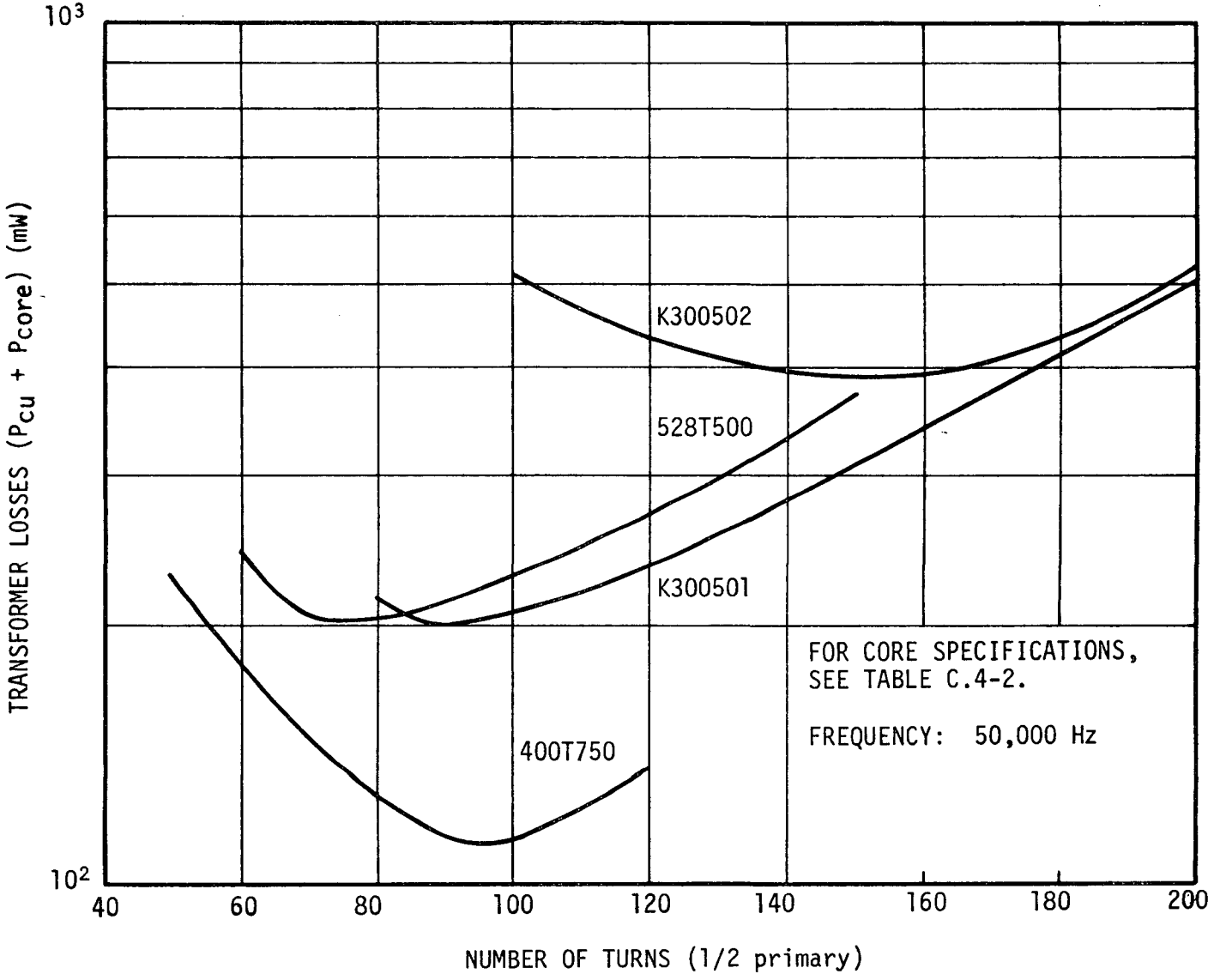


FIGURE C.4-3. LOSS CHARACTERISTICS OF VARIOUS FERRITE CORE SIZES AT 50,000 Hz

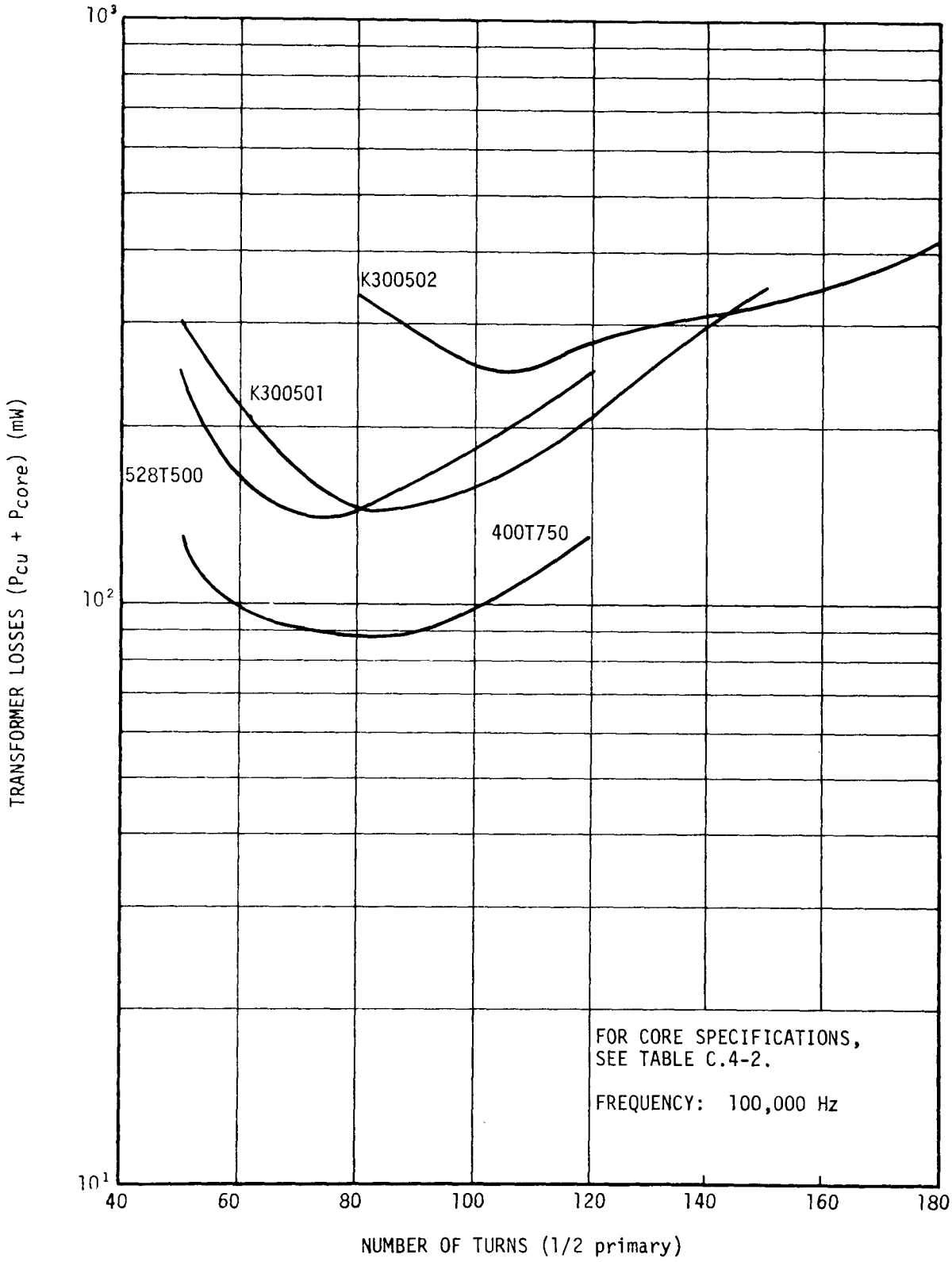


FIGURE C.4-4. LOSS CHARACTERISTICS OF VARIOUS FERRITE CORE SIZES AT 100,000 HERTZ

material. The copper losses were computed using Equation 5, given the same number of turns and core parameters. Since the entire window area is utilized for each core for a given number of turns by adjusting the wire size, the copper losses are always minimum for that number of turns.

The ferrite materials are far superior to the tape wound core using Permalloy 80 material, as can be seen in Figure C.4-1. All of the cores are approximately the same physical size.

The Permalloy 80 1.0 MIL material is better than the 0.25 MIL material for the same size cores since the stacking factor causes the effective cross sectional area to decrease significantly (see Table C.4-1).

Figures C.4-2, C.4-3, and C.4-4 show ferrite toroid cores of different sizes and at different operating frequencies (losses decrease with increasing core size and increasing frequencies).

Ferrite toroidal cores were selected for the power supply design since they afford a significant efficiency improvement over the other materials and core shapes analyzed.

Although this analysis suggests that the transformer core size be large and the operating frequency be high, since the total transformer losses decrease with increased core size and operating frequency, these design parameters are limited by the maximum size requirements for the overall power supply and by the frequency dependent losses contributed by the power switching devices. Since the overall size and efficiency of the power supply are to be optimized, consideration must be given to all of the components of the power supply with regard to their size and efficiency as a function of frequency characteristics.

TABLE C.4-1. CORES OF VARIOUS MATERIALS WHICH ARE SIZE-EQUIVALENT

ITEM	DATA
CORE NO. 1: FERRITE "E" CORE -- PART NO. 783E608*	
Type Material	3B7 (must be made in 3B7)
Winding Area	0.276 in^2
Volume	17.71 cm^3
Effective Cross Sectional Area	1.81 cm^2
Mean Length/Turn	3.66 in.
Mean Magnetic Length	9.73 cm
Length	1.646 in.
Height	1.653 in.
Width	0.608 in.
CORE NO. 2: TAPE WOUND TOROID CORE -- PART NO. 50026-1/4D**	
Type Material	Permalloy 80 1/4 MIL
Winding Area	0.660 in^2
Volume	2.0 cm^3 (core material)
Effective Cross Sectional Area	0.210 cm^2
Mean Length/Turn	2.2 in.
Mean Magnetic Length	9.97
Inside Diameter	0.915 in.
Outside Diameter	1.585 in.
Width	0.470 in.
CORE NO. 3: TAPE WOUND TOROID CORE -- PART NO. 50026-1D**	
Type Material	Permalloy 80 1.0 MIL
Winding Area	0.660 in^2
Volume	4.52 cm^3
Effective Cross Sectional Area	0.454 cm^2
Mean Length/Turn	2.2 in.
Mean Magnetic Length	9.97 cm
Inside Diameter	0.915 in.
Outside Diameter	1.585 in.
Width	0.470
CORE NO. 4: FERRITE POT CORE -- PART NO. 4229*	
Type Material	3B7
Winding Area	0.195 in^2
Volume	18.2 cm^3
Effective Cross Sectional Area	2.66 cm^2
Mean Length/Turn	3.39 in.
Mean Magnetic Length	6.81 cm
Outside Diameter	1.697 in.
Width	1.162 in.

*Manufactured by Ferroxcube, Inc. Saugerties, New York
**Manufactured by Magnetics, Inc., Butler, Pennsylvania

TABLE C.4-1. - Concluded

ITEM	DATA
CORE NO. 5: FERRITE TOROID CORE -- PART NO. 528T500*	
Type Material	3B7 (3C8)
Winding Area	0.465 in^2
Volume	10.45 cm^3
Cross Sectional Area	1.21 cm^2
Mean Length/Turn	2.2 in.
Mean Magnetic Length	8.63 cm
Outside Diameter	1.53 in.
Inside Diameter	0.770 in.
Width	0.500 in.

*Manufactured by Ferroxcube, Inc., Saugerties, New York

TABLE C.4-2. VARIOUS-SIZED FERRITE TOROID CORES

ITEM	DATA
FERRITE TOROID CORE -- PART NO. K300502*	
Type Material	3B7 (must be made in 3B7)
Winding Area	0.440 in^2
Volume	2.58 cm^3
Cross Sectional Area	0.373 cm^2
Mean Length/Turn	1.60 in.
Mean Magnetic Length	9.20 cm
Outside Diameter	1.142 in.
Inside Diameter	0.748 in.
Width	0.394 in.
FERRITE TOROID CORE -- PART NO. K300501*	
Type Material	3B7 (must be made in 3B7)
Winding Area	0.653 in^2
Volume	9.0 cm^3
Cross Sectional Area	0.977 cm^2
Mean Length/Turn	2.3 in.
Mean Magnetic Length	9.20 cm
Outside Diameter	1.417 in.
Inside Diameter	0.905 in.
Width	0.591 in.
FERRITE TOROID CORE -- PART NO. 538T500*	
Type Material	3B7 (or 3C8)
Winding Area	0.465 in^2
Volume	10.45 cm^3
Cross Sectional Area	1.21 cm^2
Mean Length/Turn	2.2 in.
Mean Magnetic Length	8.63 cm
Outside Diameter	1.53 in.
Inside Diameter	0.770 in.
Width	0.500 in.
FERRITE TOROID CORE -- PART NO. 400T750*	
Type Material	3B7 (or 3C8)
Winding Area	1.27 in^2
Volume	23.063 cm^3
Cross Sectional Area	1.81 cm^2
Mean Length/Turn	3.0 in.
Mean Magnetic Length	12.7 cm
Outside Diameter	2.040 in.
Inside Diameter	1.270 in.
Width	0.750 in.

*Manufactured by Ferroxcube, Inc., Saugerties, New York

C.5. LOSS ANALYSIS OF POWER SWITCHING DEVICES

The purpose of the analysis discussed here was to determine the major power losses contributed by semiconductor devices in the power supply.

C.5.1 POWER TRANSISTOR LOSSES

Losses in power transistors are caused primarily by four transistor parameters. These parameters, as well as the general equations which relate the parameters to power loss, are listed below.

- Rise and Fall Switching Time

$$P_{loss} = \frac{1}{2} (E_p) (I_p) \left(\frac{t_f}{T}\right) + \frac{1}{3} (E_p) (I_p) \left(\frac{t_r}{T}\right)$$

where

E_p - peak collector voltage

I_p - peak collector current

t_f - transistor fall time

t_r - transistor rise time

T - period of one cycle of operation.

- Collector Saturation Voltage

$$P_{loss} = (V_{CE_{sat}}) (I_c) \left(\frac{T_{on}}{T}\right)$$

where

$V_{CE_{sat}}$ - collector-to-emitter saturation voltage

I_c - average collector current

T_{on} - transistor on time per cycle

T - per-cycle period.

- Collector Leakage Current

$$P_{loss} = (I_{CL})(V_{CE}) \left(\frac{T_{off}}{T}\right)$$

where

I_{CL} - leakage current from collector ($\simeq I_{CEV}$)

V_{CE} - collector voltage

T_{off} - transistor off time

T - period of one cycle.

- Saturated Forward-Current Transfer Ratio

$$P_{loss} = \frac{T_{on}}{T} \left(\frac{I_C}{h_{FE_{sat}}} \cdot V_{BE_{sat}}\right) \left(\frac{1}{\text{efficiency of base drive circuit}}\right)$$

where

T_{on} - transistor on time

T - period of one cycle

I_C - collector current

$V_{BE_{sat}}$ - base-to-emitter saturation voltage

$h_{FE_{sat}}$ - saturated forward transfer ratio.

C.5.2 DIODE LOSSES

Diode losses primarily are caused by three parameters: leakage current; forward voltage drop; and reverse recovery time. The equations which relate these parameters to loss are:

- Forward Voltage Drop

$$P_{loss} = (I_F)\,(V_F)\left(\frac{T_{on}}{T}\right)$$

where

I_F - average forward current

V_F - forward voltage drop

T_{on} - conduction time per cycle

T - period of one cycle.

- Leakage Current

$$P_{loss} = (I_R)\,(V_R)\left(\frac{T_{off}}{T}\right)$$

where

I_R - reverse voltage leakage current

V_R - reverse voltage

T_{off} - off time per cycle

T - period of one cycle

- Reverse Recovery Time

$$P_{loss} = \left(\frac{V_R^{\,2}}{L_\ell}\right)\left(\frac{t_{rr}^{\,2}}{3T}\right)$$

where

V_R - reverse voltage

L_ℓ - secondary leakage inductance of power transformer

t_{rr} - reverse recovery time

T - period of one cycle.

This equation is an approximation valid for conditions where the driving impedance is low and where the major current determining factor is the transformer secondary leakage inductance.

Figure C.5-1 shows a plot of these losses as a function of frequency for a state-of-the-art, high-speed, triple-diffused transistor and a Schottky barrier diode. These devices are typical of those used in the power supply when it is delivering 50 watts at 5 volts, dc.

C.5.3 CONCLUSIONS

The two most significant losses associated with the switching devices in the power supply are attributed to the power diode conduction losses and the power switching transistor switching losses. The diode losses, which are frequency dependent, diode reverse recovery losses, do not become appreciable until the frequency is increased beyond approximately 70 kilohertz. The transistor frequency dependent losses, however, become significant beyond 5 kilohertz. In order to meet the requirement that the power supply will be 85 percent efficient dictates that the operating frequency must not be in excess of approximately 20 kilohertz. At 20 kilohertz the total diode and transistor losses for two diodes and two transistors are equal to 6.2 watts (Figure C.5-1). For a 50-watt power supply to be 85 percent efficient, the total power loss must be equal to or less than 8.8 watts. This allows 2.6 watts of additional power to be used for the control circuitry, the base drive circuitry, and dissipated in the input and output filters.

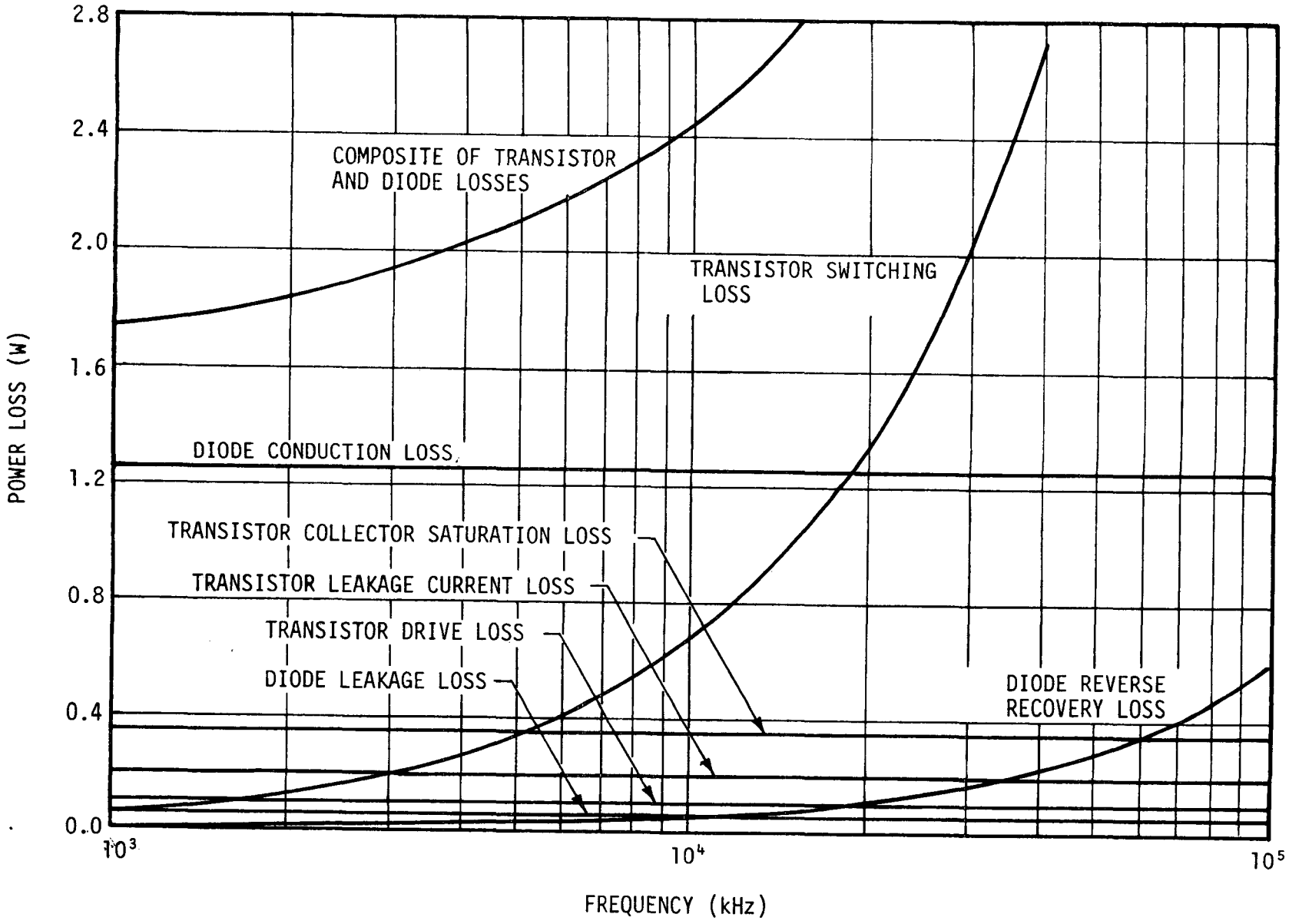


FIGURE C.5-1. DIODE AND TRANSISTOR LOSSES AS A FUNCTION OF OPERATING FREQUENCY

C.6. ANALYSIS OF TRANSISTOR PERFORMANCE CHARACTERISTIC AS RELATED TO BASE DRIVE

The purpose of this discussion was to determine the relationship between transistor performance and the magnitude of transistor base drive.

C.6.1 SATURATION VOLTAGE

Under conditions of saturation, the voltage drop between collector and emitter and base to emitter can be expressed as

$$V_{CE} = R_C I_C + \frac{\eta K T}{q} \ln \frac{\alpha_I \left[1 - \frac{I_C}{I_B} \frac{(1 - \alpha N)}{\alpha N} \right]}{1 + \frac{I_C}{I_B} \left(1 - \alpha_I \right)}$$

$$V_{BE} = I_B r_{bb'} + \frac{\eta K T}{q} \ln \left(1 - \frac{I_E + \alpha_I I_C}{I_{EO}} \right)$$

where

V_{CE} - collector-to-emitter voltage

V_{BE} - base-to-emitter voltage

R_C - ohmic resistance from collector to emitter

I_C - collector current

η - constant of value between 1 and 2, depending on characteristic of the transistor material

K - Boltzmann's constant = 1.38×10^{-28} W·sec/°C

T - absolute temperature, °K

q - electronic charge = 1.60×10^{-19} coulomb

I_B - base current

I_E - emitter current

I_{EO} - emitter leakage current with reverse voltage applied to the emitter, and collector open-circuited

$r_{bb'}$ - ohmic base resistance

α_I - dc common base reverse current transfer ratio

α_N - dc common base forward current transfer ratio .

These relationships of collector-to-emitter and base-to-emitter voltage are complex since α_N and α_I vary with collector and emitter current, making them unusable in detail design. Optimization may be performed, however, by using manufacturers' data of collector-to-emitter saturation and base-to-emitter saturation voltage.

From these data, a curve representing saturation losses ($V_{CE} \times I_C$) and base drive losses ($V_{BE} \times I_B$) may be generated and an optimum base drive can be determined. This point, the point at which the sum of the base loss plus collect saturation loss is a minimum, specifies the relationship between collector current and base current (the ratio of I_C/I_B).

C.6.2 RISE SWITCHING TIME

Transistor rise time (from 0 to 100 percent of the on-collector current) may be expressed as

$$t_r = h_{FE}\left(\frac{1}{\omega_T} + C_C R_C\right) \ell n \frac{\frac{h_{FE} I_{B1}}{I_{CS}}}{\frac{h_{FE} I_{B1}}{I_{CS}} - 0.9}$$

which reduces to

$$t_r \cong 0.9\left(\frac{1}{\omega_T} + C_C R_C\right)\left(\frac{I_{CS}}{I_{B1}}\right)$$

when

$$\frac{h_{FE}\, I_{B1}}{I_{CS}} >> 1$$

where

t_r - rise time (from 0 to 100 percent of I_{CS})

h_{FE} - dc forward transfer ratio

I_{B1} - actual base current

I_{CS} - saturation collector current

ω_T - radian frequency at which the current gain is unity

C_C - collector transition capacitance (C_{0b})

R_C - collector saturation resistance ($R_C = V_{CC}/I_{CS}$) .

It may be noted that for the condition of heavy overdrive [$(h_{FE}\, I_{B1})/I_{CS} >> 1$] the rise time is independent of h_{FE}. For this reason, and because the rise time varies inversely with I_{B1}, it is advantageous to drive a transistor well into saturation with a large base current to minimize rise time.

C.6.3 FALL SWITCHING TIME

Transistor fall time (for 100 percent to 0 percent of the on-collector current) may be expressed as

$$t_f = h_{FE}\left(\frac{1}{\omega_T} + C_C\, R_C\right) \ln \frac{\left(1 - \frac{h_{FE}\, I_{B2}}{I_{CS}}\right)}{\left(0.1 - \frac{h_{FE}\, I_{B2}}{I_{CS}}\right)}$$

which reduces to

$$t_f = 0.9 \left(\frac{1}{\omega_T} + C_C R_C\right)\left(\frac{I_{CS}}{I_{B2}}\right)$$

when

$$\frac{-h_{FE} I_{B2}}{I_{CS}} >> 1$$

where I_{B2} is the base current in the reverse direction. For large overdrives, the fall time is greatly affected by the reverse base drive and is independent of h_{FE}.

C.6.4 STORAGE TIME

Transistor storage time, which is the time from the occurrence of the end of the drive signal to the time when the collector current begins to change, may be expressed as

$$t_S = \left[\frac{\omega_N + \omega_I}{\omega_N \omega_I \left(1 - \alpha_{NO} \alpha_{IO}\right)}\right] \ell n \frac{I_{B1} - I_{B2}}{I_{BA} - I_{B2}}$$

where

ω_N - the radian frequency at which the low frequency forward current gain is -3 decibels

ω_I - the radian frequency at which the low frequency reverse current gain is -3 decibels

α_{NO} - low frequency forward current gain

α_{IO} - low frequency reverse current gain

I_{B1} - base current before turnoff

I_{B2} - reverse base current at turnoff

I_{BA} - magnitude of the base current in order to just enter saturation ($I_{BA} = I_{CS}/h_{FE}$).

Although storage time does not contribute to any loss, it is important to realize that storage time limits the minimum time the transistor can be "on" if saturated. This may limit the minimum duty cycle and can be minimized by providing a large reverse base current and/or reducing the forward base drive.

C.6.5 DELAY SWITCHING TIME

Transistor delay time, which is the time required for a transistor to be brought from cutoff to the active region, may be expressed as

$$t_d = R_S' (C_{ib} + C_{ob}) \ell n \frac{V_1 - V_2}{V_1 - V_\gamma} + \frac{1}{6\pi f_T}$$

where

t_d - delay time

R_S' - total base circuit impedance including the intrinsic base resistance

C_{ib} - common base input transition capacitance

C_{ob} - collector transition capacitance

V_1 - forward base drive voltage

V_2 - reverse base voltage

V_γ - forward cut-in voltage (0.5V for Si)

f_T - common emitter gain-bandwidth product.

Delay time, as shown in the above expression, may be minimized by keeping the reverse voltage low during turn-off and/or by driving the base with a large forward voltage during turn-on.

C.6.6 DISCUSSION

The switching parameters of transistors, except for delay time, are directly related to the magnitudes of the forward and reverse base currents. These performance parameters being base drive current related rather than base voltage related indicates that a current mode drive scheme be used rather than voltage drive. The single most efficient means of providing current mode drive would be to use a current mode transformer to maintain a fixed forced beta with an additional winding added for control. The control winding must be driven so as to provide a turn-on current independent of the base-to-emitter voltage of the power transistor, minimizing rise time and delay time. The circuit also must be able to supply relatively large reverse current during the off-transition time to minimize fall time, storage time, and losses during transistor cutoff.

C.7. ANALYSIS OF REQUIREMENTS FOR THE INPUT FILTER

The purpose of this analysis was to determine the specific requirements for the individual input components of a single-stage, LC type filter and to utilize this data to optimize the input filter design.

C.7.1 CAPACITOR DESIGN REQUIREMENTS

RMS Ripple Current

The rms ripple current impressed across the input capacitor(s) of the regulator can be calculated from the current waveform looking into the power supply (see Figure C.7-1). This waveform was derived from the input filter simplified schematic shown in Figure C.7-2.

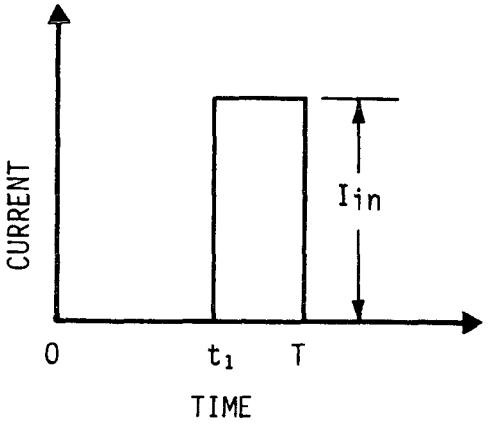


FIGURE C.7-1. POWER SUPPLY INPUT CURRENT WAVEFORM

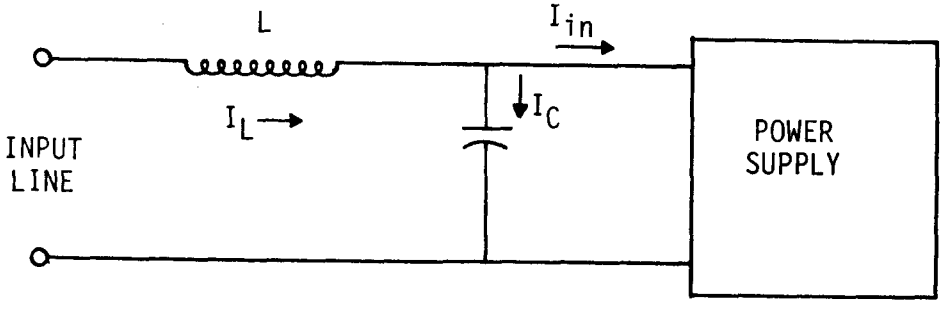


FIGURE C.7-2. INPUT FILTER SIMPLIFIED SCHEMATIC

In Figure C.7-1, "T" is the period of the repetitive input current waveform, which is equal to one-half the operating frequency of the power supply since the inverter operates in a push-pull manner. The time represented by t_1 to T is the time the power supply draws input current; e.g., the period during which one of the power transistors in the inverter is conducting. During the 0 to t_1, neither transistor conducts; therefore, current does not flow during this interval.

Since the energy into the supply must equal the energy going out plus losses, we may write

$$\int_0^T (E_{in})(I_{in})dt = \frac{P_{out}}{\eta} T \quad .$$

Since I_{in} is 0 for $0 < t < t_1$, then

$$E_{in} I_{in} (T - t_1) = \frac{P_{out} T}{\eta}$$

and

$$I_{in} = \frac{P_{out}}{E_{in} \eta} \left(\frac{T}{T - t_1}\right)$$

where

P_{out} - output power

E_{in} - input voltage

η - efficiency of the power supply

I_{in} - input current for the power supply.

However, since the input choke supplies current during the total time (0 to T) and since this current has an extremely small ripple current component, it may be considered constant and equal to the average input current, as

$$I_L = \frac{P_{out}}{E_{in}\,\eta}$$

where I_L is the current supplied by the input choke.

Since the choke current (I_L) is supplied during the total time, the capacitor current must be the difference between the required current and the choke current, as

$$I_C\,(0 < t < t_1) = I_L = \frac{P_{out}}{E_{in}\,\eta}$$

$$I_C(t < t_1 < T) = -I_{in} + I_L$$

$$= \frac{-P_{out}}{E_{in}\,\eta}\left(\frac{T}{T - t}\right) + \frac{P_{out}}{E_{in}\,\eta}$$

and

$$-I_C = \frac{P_{out}}{E_{in}\,\eta}\left(\frac{t_1}{T - t_1}\right)$$

where

I_L - inductor current

I_C - capacitor current.

The composite waveform is shown in Figure C.7-3.

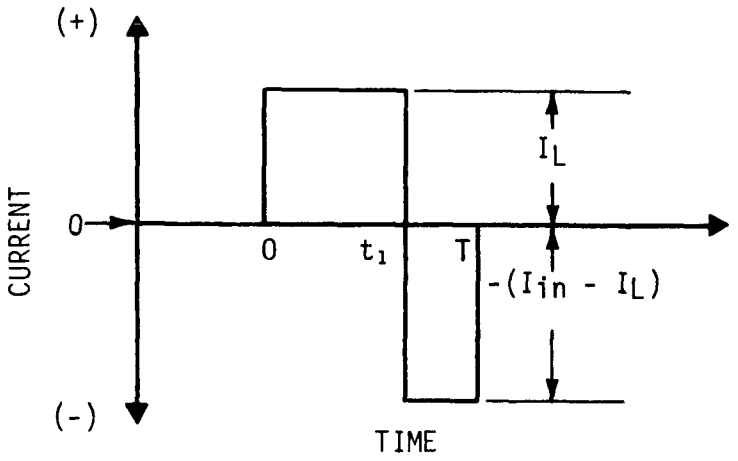


FIGURE C.7-3. CAPACITOR RIPPLE CURRENT WAVEFORM

From these relationships, the rms capacitor current can be calculated

$$I_{C(rms)} = \left[\frac{1}{T}\int_0^T f(t)^2\,dt\right]^{\frac{1}{2}}$$

$$I_{C(rms)} = \left[\frac{1}{T}\int_0^{t_1}\left(\frac{P_{out}}{E_{in}\,\eta}\right)^2 dt + \frac{1}{T}\int_{t_1}^{T}\left(\frac{P_{out}}{E_{in}\,\eta}\right)^2\left(\frac{t_1}{T - t_1}\right)^2 dt\right]^{\frac{1}{2}}$$

$$= \left\{\frac{1}{T}\left(\frac{P_{out}}{E_{in}\,\eta}\right)^2\left[t_1 + \frac{t_1^{\,2}\,T}{(T - t_1)^2} - \frac{t_1^{\,3}}{(T - t_1)^2}\right]\right\}^{\frac{1}{2}}$$

$$= \left[\left(\frac{P_{out}}{E_{in}\,\eta}\right)^2\left(\frac{t_1}{T - t_1}\right)\right]^{\frac{1}{2}} = \frac{P_{out}}{E_{in}\,\eta}\left(\frac{t_1}{T - t_1}\right)^{\frac{1}{2}}$$

where $I_{C(rms)}$ is the rms capacitor current..

Also, since the duty cycle $[(T - t_1)/(T)]$ can be expressed as a ratio of the input-to-output voltage, as

$$\frac{T - t_1}{T} = \frac{K E_{out}}{E_{in} \eta}$$

where

$\frac{T - t_1}{T}$ - duty cycle $= \frac{\text{(On time)}}{\text{(Total time)}}$

E_{out} - output voltage

E_{in} - input voltage

η - efficiency of the power supply

K - output-to-input turns ratio of the power transformer.

we may write the relationship of $(t_1)/(T - t_1)$ also in terms of E_{out} and E_{in}, as

$$\frac{t_1}{T - t_1} = \frac{E_{in} \eta}{K E_{out}} - 1 \quad .$$

Since

$$I_{C(rms)} = \frac{P_{out}}{E_{in} \eta} \left(\frac{t_1}{T - t_1} \right)^{\frac{1}{2}}$$

then

$$I_{rms} = \frac{P_{out}}{E_{in} \eta} \left(\frac{E_{in} \eta}{K E_{out}} - 1 \right)^{\frac{1}{2}} \quad .$$

The worst-case efficiency (approximately 80 percent) occurs at the lowest value of output voltage (approximately 4.0 Vdc), which represents a transformer turns ratio of approximately 9 to 1. The worst-case rms current may be calculated as

$$I_{rms_{(worst\ case)}} = \frac{P_{out}}{(0.8)(6)} \left(\frac{0.8\ E_{in} - 36}{E_{in}^2} \right)^{\frac{1}{2}}$$

maximizing the term in the radical

$$I_{rms_{(worst\ case)}} = \frac{P_{out}}{72} \quad .$$

Peak-to-Peak Capacitor Ripple Current

From Figure C.7-3, the peak-to-peak ripple current may be expressed as

$$I_{p\text{-}p} = I_L + I_{in} - I_L = I_{in} \quad .$$

Substituting for I_{in},

$$I_{p\text{-}p} = \frac{P_{out}}{E_{in}\,\eta} \left(\frac{T}{T - t_1} \right)$$

and can be written as

$$I_{p\text{-}p} = \frac{P_{out}}{E_{in}\,\eta} \left(\frac{E_{in}\,\eta}{K\,E_{out}} \right) \quad ;$$

thus

$$I_{p\text{-}p} = \frac{P_{out}}{K\, E_{out}} \quad .$$

Maximizing ($K = 9$, $E_{out} = 4.0$ V),

$$I_{p\text{-}p(\text{worst case})} = \frac{P_{out}}{36} \quad .$$

Voltage and Operating Temperature Requirement

The maximum voltage and operating requirements of the input capacitors are defined in the preliminary specification shown in Appendix A. In summary, they are defined by the maximum input voltage plus the worst-case input voltage transient and by the operating and storage temperature of the power supply, or:

- Operating Voltage Range: 200 volts maximum
- Operating Temperature: +85°C maximum
- Storage Temperature: +100°C maximum .

C.7.2 INDUCTOR DESIGN REQUIREMENTS

General Requirements

The inductance requirement for the input choke can be defined from the relation:

$$L \frac{di}{dt} = E$$

where

L - inductance

E - voltage across the inductor

di/dt - rate of change of inductor current.

Since the voltage (E) impressed across the inductor is that ripple voltage which appears across the filter capacitor, this voltage may be derived from the equivalent series resistance of the capacitor and the peak-to-peak current flowing through the capacitor, as

$$E_{p\text{-}p} = \overbrace{\frac{1}{C}\int_0^t i_c\,dt}^{\text{Term 1}} + \overbrace{R_c \cdot I_{p\text{-}p}}^{\text{Term 2}}$$

where

$E_{p\text{-}p}$ - peak-to-peak ripple voltage

C - capacitance

i_c - capacitor current

R_c - capacitor equivalent series resistance

$I_{p\text{-}p}$ - capacitor peak-to-peak ripple current.

Term 1 in the above equation represents the effects of charging and discharging the capacitor. Since the amount of energy transfered during the charging interval is equal to the amount of energy lost in the capacitor during the discharge interval, then

$$\frac{1}{C}\int_0^{t_1} i_c(t)\,dt = \frac{1}{C}\int_{t_1}^{T} i_c(t)\,dt$$

$$\frac{1}{C}\int_0^{t_1} i_c(t)\,dt = \frac{1}{C}\left(\frac{P_{out}}{E_{in}\,\eta}\right) t_1$$

where

$0 < t < t_1$ - the interval when both inverter transistors are off

$t_1 < t < T$ - the interval during which one of the inverter transistors is on

T - one-half the period of the operating frequency of the inverter (the inverter operates push-pull)

C - capacitance of capacitor

i_c - capacitor current

P_{out} - output power

E_{in} - input voltage

η - efficiency of the power supply.

Since the duty cycle $\left(\frac{T - t_1}{T}\right)$ can be represented as a ratio of the input-to-output voltage, as

$$\frac{T - t_1}{T} = \frac{K E_{out}}{E_{in} \eta}$$

and

$$t_1 = \left(1 - \frac{K E_{out}}{E_{in} \eta}\right) T$$

where

K - output transformer turns ratio

E_{out} - output voltage

then

$$\frac{1}{C} \int_0^{t_1} i_c(t)\, dt = \frac{1}{C} \frac{P_{out}}{E_{in} \eta} \left(1 - \frac{K E_{out}}{E_{in} \eta}\right) T .$$

Maximizing for a worst case (lowest efficiency, lowest output voltage), when K = 9, E_{out} = 4.0 volts, and η = 80 percent, then

$$\frac{1}{C}\int_0^{t_1} i_c(t)\,dt = \frac{1}{C}\left(\frac{P_{out}}{144}\right) T \quad .$$

Since the worst case peak-to-peak ripple current (I_{p-p}) is equal to $P_{out}/36$ (see page C.7-7), the worst-case peak-to-peak ripple voltage may be written as

$$E_{p-p} = \frac{1}{C}\left(\frac{P_{out}}{144}\right) T + R_c\left(\frac{P_{out}}{36}\right)$$

$$E_{p-p} = P_{out}\left(\frac{T}{144\,C} + \frac{R_c}{36}\right)$$

The approximate waveshape of this ripple voltage is shown in Figure C.7-4.

A safe assumption is that the ripple voltage is a square wave, which is the worst-case amplitude of the fundamental frequency. Therefore, the inductance of the choke may be calculated from

$$L\,\frac{di}{dt} = E_{p-p} = \text{constant}$$

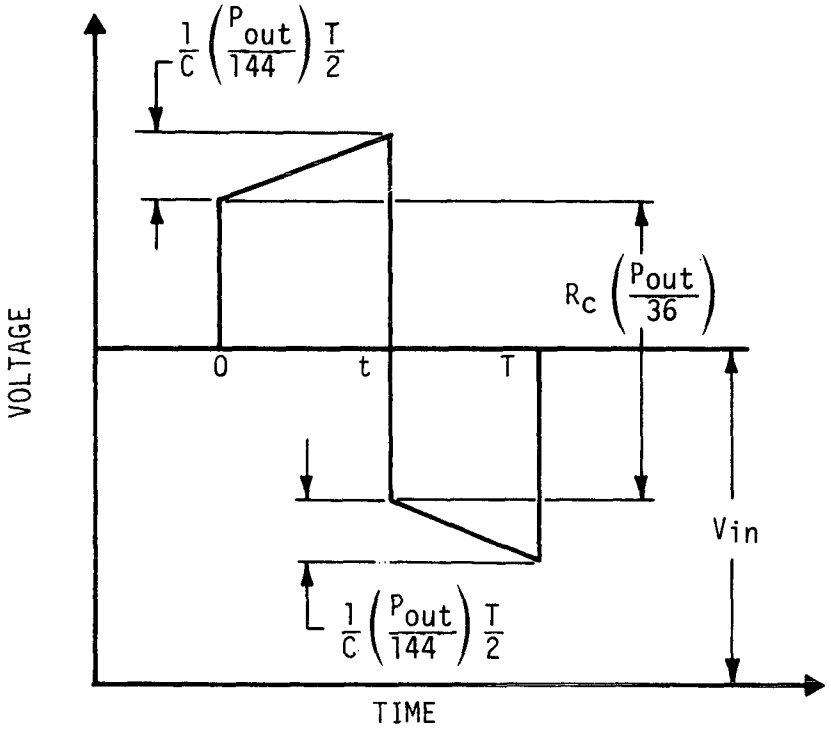


FIGURE C.7-4. WAVEFORM FOR THE CAPACITOR RIPPLE VOLTAGE

$$di = \frac{E_{p-p}}{L}\int_0^t dt$$

$$\Delta i = \frac{E_{p-p}}{L}\, t$$

where

E_{p-p} - worst-case peak-to-peak ripple voltage

t - T/2

L - inductance required

Δi - peak-to-peak input ripple current (approximately a triangular wave) which is specified by MIL SPEC 461-A for frequency $\frac{1}{T}$.

The only other electrical requirement for the inductor is that it be capable of supporting a dc current equal to the peak input current without saturating. That is,

$$B_{SAT} = \mu H > \left(\frac{0.4\pi N I_p}{m_\ell}\right) \mu$$

where

B_{SAT} - saturation flux density of the core material used

μ - permeability of the core

N - number of turns on the core

I_p - peak choke current which is equal to the average input current plus ripple ($\sim P_o/E_{in}\,\eta$)

m_ℓ - mean magnetic path-length of the core.

Size, Weight, and Efficiency Considerations

The inductance required for the input choke can be defined as follows. Given core parameters, the number of turns required can be calculated by

$$N^2 = \frac{L\, m_\ell}{0.4\,\pi\, A\, \mu} \times 10^8$$

where

N - number of turns

L - inductance required (henrys)

m_ℓ - magnetic length of the core (cm)

A - core cross-sectional area (cm^2)

μ - core permeability.

Also, since the core must not saturate, an additional requirement is imposed. Since:

$$H = \frac{0.4\,\pi\,NI}{m_\ell}$$

then

$$B_{SAT} = \mu\,H_s \geq \left(\frac{0.4\,\pi\,NI_p}{m_\ell}\right)\mu$$

where

B_{SAT} - satuation flux density (gausses)

I_p - peak choke current

H_s - magnetizing force (oersteds) at which saturation occurs at a given permeability

H - magnetizing force (oersteds)

If

$$B_{SAT} = \frac{0.4\,\pi\,N\,I_p}{m_\ell}\ (\mu)$$

rearranging

$$N = \frac{B_{SAT}\,m_\ell}{0.4\,\pi\,I_p\,\mu}$$

and the value of N (number of turns) becomes the maximum number of turns which the core can support. Given a core, the magnetic length, cross-sectional area, maximum flux density, and fixed peak current, the only parameter that can be varied to increase the number of turns allowable is the permeability (μ). Since the number of turns required is

$$N^2 = \frac{L\, m_\ell}{0.4\,\pi\, A\,\mu} \times 10^8 \quad ,$$

reducing the permeability increases the number of turns required. Also,

$$N = \frac{H\, m_\ell}{0.4\,\pi\, I_p}$$

and

$$L = \frac{0.4\,\pi\, N^2\,\mu\, A}{m_\ell} \times 10^{-8} \quad .$$

Substituting for N in the last equation,

$$L = \frac{0.4\,\pi\, N}{m_\ell}\left(\frac{H\, m_\ell}{0.4\,\pi\, I_p}\right)\mu\, A \times 10^{-8}$$

becomes

$$L\, I_p = \mu\, H\, (NA) \times 10^{-8} \quad .$$

If both sides are multiplied by $\left(\frac{I_p}{2}\right)$, and noting that $\mu\, H = B$,

then

$$\frac{1}{2}\, L\, I_p^2 = B\, (NI_p)\, A \times 10^{-8} \quad .$$

Since

$$N\, I_p\, \alpha\, \frac{m_\ell}{\mu}$$

then

$$\frac{1}{2}\, L\, I_p = \text{Energy Stored}\, \alpha\, \frac{A\, m_\ell}{\mu} = \frac{\text{Core Volume}}{\mu} \quad .$$

Therefore, the maximum energy storage capability of a core is directly related to volume and inversely related to permeability. However,

since the core window area (W_a) can be related to mean magnetic length for an optimized core design, window area becomes a function of core volume. This, combined with the fact that copper losses are directly related to the number of turns squared and window area, as

$$P_{copper} \alpha \frac{N^2}{W_a} \text{ (Ref. Appendix C. 4),}$$

shows that decreasing the permeability increases the number of turns and the copper loss, the latter in direct proportion.

Since the direct current is much larger than the ripple current in the choke, the copper losses, in low-loss materials such as in ferrite and powdered permalloy cores, are the determining factors affecting efficiency. Therefore, choke weight and volume can be reduced only if efficiency is degraded.

C. 7. 3 CONCLUSIONS

The selection of a high performance input filter capacitor is essential in the design of the input filter since it governs the design of the filter choke. These performance characteristics are summarized below:

- They must be able to withstand the required rms ripple currents in order to be reliable.
- They must have high capacitance-voltage products to minimize size and weight.
- They must exhibit low impedance at the operating frequency to minimize size and weight of the filter choke.

These performance requirements dictate the use of tantalum capacitors which were selected for the design.

Since there is a direct relationship between choke size and efficiency, once the input filter capacitor parameters are defined, the input choke can then be readily designed based on these capacitor parameters and the required filter efficiency.

C.8. ANALYSIS OF REQUIREMENTS FOR THE OUTPUT FILTER

The purpose of this discussion was to determine the requirements of the power supply output filter network such that an optimum design could be selected.

C.8.1 GENERAL REQUIREMENTS

The requirements for the output filter can be determined readily by constructing a general schematic (Figure C.8-1) and analyzing the current and voltage waveforms produced. These waveforms are shown in Figure C.8-2.

C.8.2 INDUCTOR ANALYSIS

The value of the required inductance may be derived as follows. Since

$$e_L = L \frac{di_L}{dt}$$

$$\int e_L \, dt = L \int di_L$$

$$\int_0^{t_{on}} \left(\frac{E_{in}}{N_R} - V_D - E_{out} \right) dt = L \int_{I_{min}}^{I_{max}} di$$

$$\left(\frac{E_{in}}{N_R} - V_D - E_{out} \right) t_{on} = L(I_{max} - I_{min}) = L\Delta i \qquad (1)$$

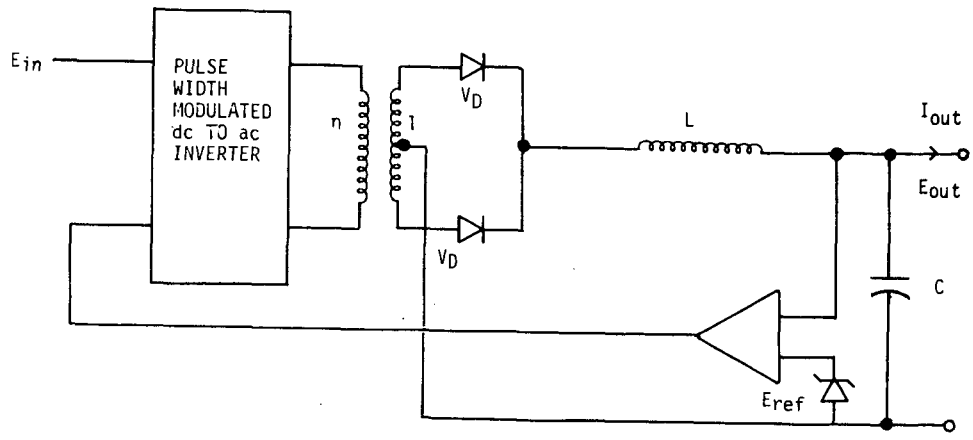
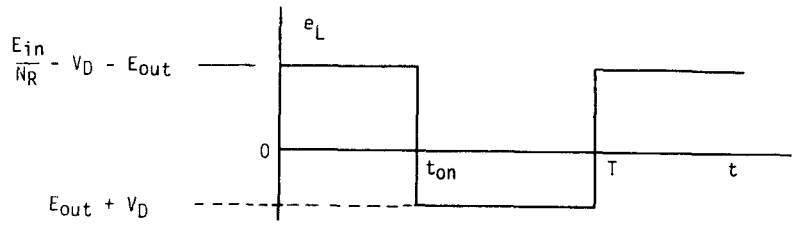
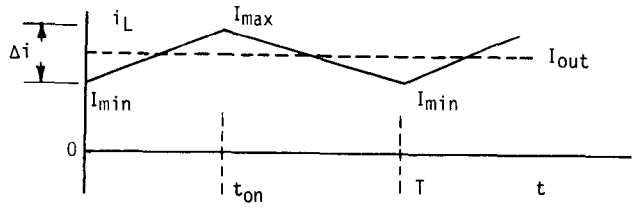


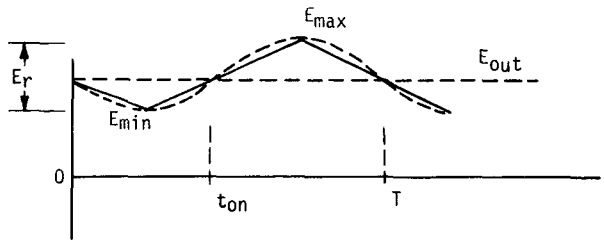
FIGURE C.8-1. REGULATOR MODEL



(a) VOLTAGE WAVEFORM ACROSS INDUCTOR



(b) CURRENT WAVEFORM THROUGH INDUCTOR



(c) OUTPUT VOLTAGE WAVEFORM

NOTE:

I_{out} - OUTPUT LOAD CURRENT
E_{out} - OUTPUT VOLTAGE
Ein - INPUT VOLTAGE
N_R - TURNS RATIO OF OUTPUT TRANSFORMER

FIGURE C.8-2. CURRENT AND VOLTAGE WAVEFORMS FOR OUTPUT FILTER

and

$$\int_{t_{on}}^{T} -(E_{out} + V_D)\, dt = L \int_{I_{max}}^{I_{min}} di$$

$$(E_{out} + V_D)(T - t_{on}) = L\Delta i \qquad (2)$$

then, from Equations 1 and 2 above,

$$\left(\frac{E_{in}}{N_R} - V_D - E_{out}\right) t_{on} = (E_{out} + V_D)(T - t_{on}) \qquad (3)$$

$$\frac{t_{on}}{T} = K = N_R \frac{(E_{out} + V_D)}{E_{in}} \qquad (4)$$

where K is the duty cycle. From Equation 2, then

$$(E_{out} + V_D)\, T \left[1 - \frac{N(E_{out} + V_D)}{E_{in}}\right] = L\Delta i \qquad (5)$$

and solving for the inductance,

$$L = \frac{E_{out} + V_D}{\Delta i \cdot f} \left[1 - \frac{N_R (E_{out} + V_D)}{E_{in}}\right] . \qquad (6)$$

The value of inductance variations is investigated in Figure C.8-3 for worst-case conditions.

The inductance and capacitance have been defined in terms of new parameter $R_o = (E_{out})/(I_{out})$ which simplifies design and a large number of calculations.

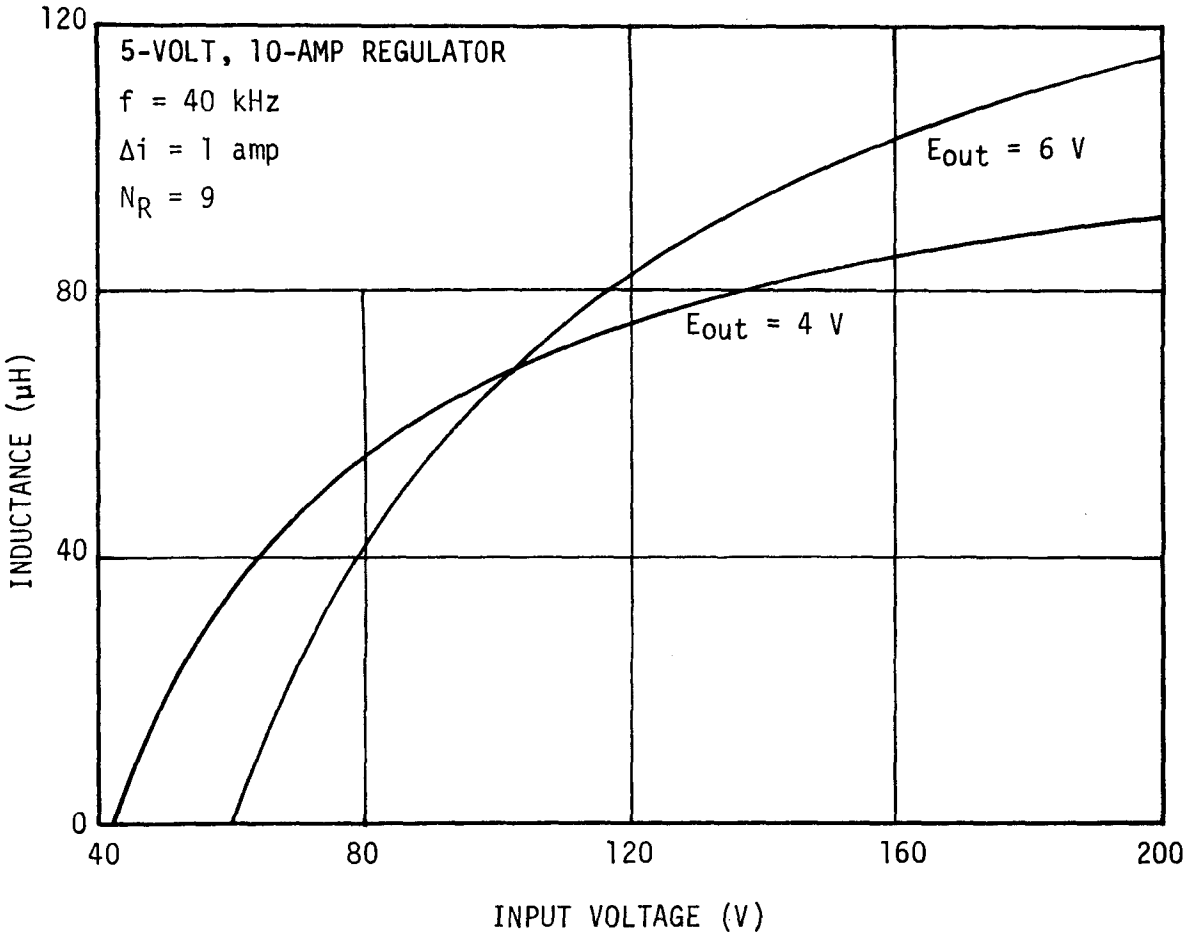


FIGURE C.8-3. INPUT LINE VOLTAGE VARIATIONS AS A FUNCTION OF INDUCTANCE

Rewriting Equations 5 and 6, and setting the ripple current (Δi) equal to 10 percent of the output load current (I_{out}),

$$L = \frac{E_{out}}{\Delta i \cdot f}(1 - K)$$

$$= \frac{10\, E_{out}}{I_{out}\, f}(1 - K)$$

$$= \frac{10\, R_o}{f}(1 - K)$$

$$L = \frac{10\, \alpha\, R_o}{f}(1 - K)$$

where α (1.2 to 1.5) is a factor to account for conductance variations due to temperature duty cycle, etc, and

$$L = \frac{(E_{out} + V_D)}{\Delta i \cdot f}\left[1 - \frac{N_R(E_{out} + V_D)}{E_{in}}\right]. \qquad (7)$$

Then for $E_{out} >> V_D$, the value of inductance becomes

$$L = \frac{E_{out}}{\Delta i \cdot f}(1 - K) \quad . \qquad (8)$$

A curve representing the value of inductance required as a function of output voltage is shown in Figure C.8-3.

C. 8. 3 CAPACITOR ANALYSIS

The value of the required capacitance (C) may be derived as follows: Since

$$\Delta i = C \frac{d V_r}{dt}$$

$$C = \frac{\int \Delta i \, dt}{\int dV_r}$$

$$C = \frac{\int_{t_{on}/2}^{t_{off}/2} i_r \, dt}{\int_{E_{min}}^{E_{max}} dV_r}$$

where

i_r - ripple current

V_r - ripple voltage

t_{off} - time off = T - t_{on}

t_{on} - time on

and

$$C = \frac{\frac{1}{2}\left(\frac{\Delta i}{2} \cdot \frac{t_{on}}{2}\right) + \frac{1}{2}\left(\frac{\Delta i}{2} \cdot \frac{t_{off}}{2}\right)}{E_r}$$

$$C = \frac{\Delta i}{8 E_r} \left(t_{on} + t_{off}\right) .$$

Noting that $(t_{on} + t_{off}) = T = 1/f$, where f is two times the converter operating frequency, then

$$C = \frac{\Delta i}{8 f E_r} \quad . \tag{9}$$

A graph representing compatible inductance and capacitance values as a function of output impedance is shown in Figure C.8-4.

C.8.4 INDUCTOR CONSIDERATIONS

Given a core at a fixed frequency, the maximum energy storage capability is determined by the magnetic material and operating flux density of the material. The selection of the core, magnetic material, and operating flux density is simplified if normalized parameters are used. Since

$$L = \frac{0.4\pi N^2 A \mu}{m_\ell} \times 10^{-8} \text{ H} \tag{10}$$

and

$$H = \frac{0.4\pi N I}{m_\ell}$$

substituting the value of L from Equation 10

$$\frac{10\alpha R_o}{f}(1 - K) = \frac{0.4\pi N^2 A\mu}{m_\ell} \times 10^{-8}$$

$$N^2 A/m_\ell = \frac{10\alpha R_o(1 - K)\, 10^8}{0.4\pi \mu f} \quad .$$

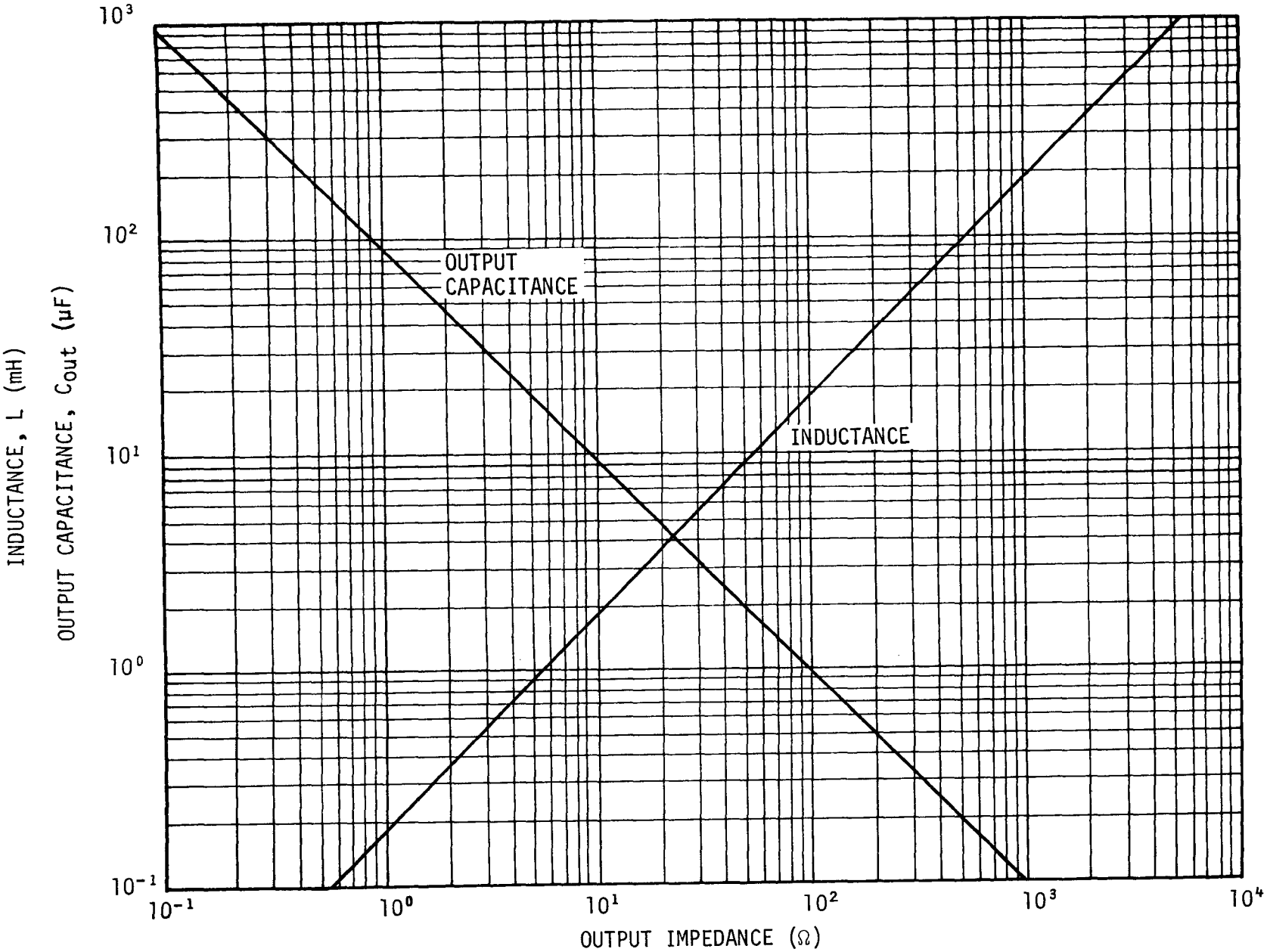


FIGURE C.8-4. CAPACITANCE-INDUCTANCE AS A FUNCTION OF OUTPUT IMPEDANCE MONOGRAPH

Define core parameter $C_2 = A/m_\ell$,

$$N_n = N/C_2)^{\frac{1}{2}} = \left(\frac{10\,\alpha\, R_o(1 - K)\, 10^8}{0.4\,\pi\,\mu\, f}\right)^{\frac{1}{2}} \qquad (11)$$

where

N - number of turns

I - magnetizing current

L - inductance

H - magnetizing force, oersteds

R_o - output impedance, ohms

μ - permeability of the core material

A - cross-section area of core

m_ℓ - magnetic path length of the core

f = 1/T

K - duty cycle.

Substituting the value of N in the expression for H

$$H = \frac{0.4\pi\, I_{out}}{m_\ell} \cdot \left[\frac{10\alpha\, R_o(1 - K)\, 10^8}{0.4\pi\,\mu\, f} \cdot \frac{m_\ell}{A}\right]^{\frac{1}{2}}$$

$$B = \mu H = \frac{0.4\pi\, I_{out}\,\mu}{m_\ell}\left[\frac{10\alpha\, E_{out}(1 - K)\, 10^8}{0.4\pi\,\mu f} \cdot \frac{m_\ell}{A}\right]^{\frac{1}{2}}$$

$$= \left[\frac{0.4\pi\,\alpha\,\mu\, P_{out}(1 - K)\, 10}{f(A\, m_\ell)}\right]^{\frac{1}{2}} .$$

Define core parameter $C_1 = A\, m_\ell$

where

A - core area

m_ℓ - mean magnetic length

$$B_n = B(C_1)^{\frac{1}{2}} = \left[\frac{0.4\pi\,\alpha\,\mu\ P_{out}(1 - K)\ 10^8}{f}\right]^{\frac{1}{2}} . \quad (12)$$

Normalized flux density, B_n, and normalized number of turns, N_n, are plotted in Figures C.8-5 and C.8-6, respectively, for different core materials. The most important result of the above analysis is that flux density depends upon output power and is independent of voltage and currents, while the number of turns depends upon the output impedance only. Knowing P_{out} and R_o, a core can be completely defined in terms of core parameters C_1 and C_2 and thus selected.

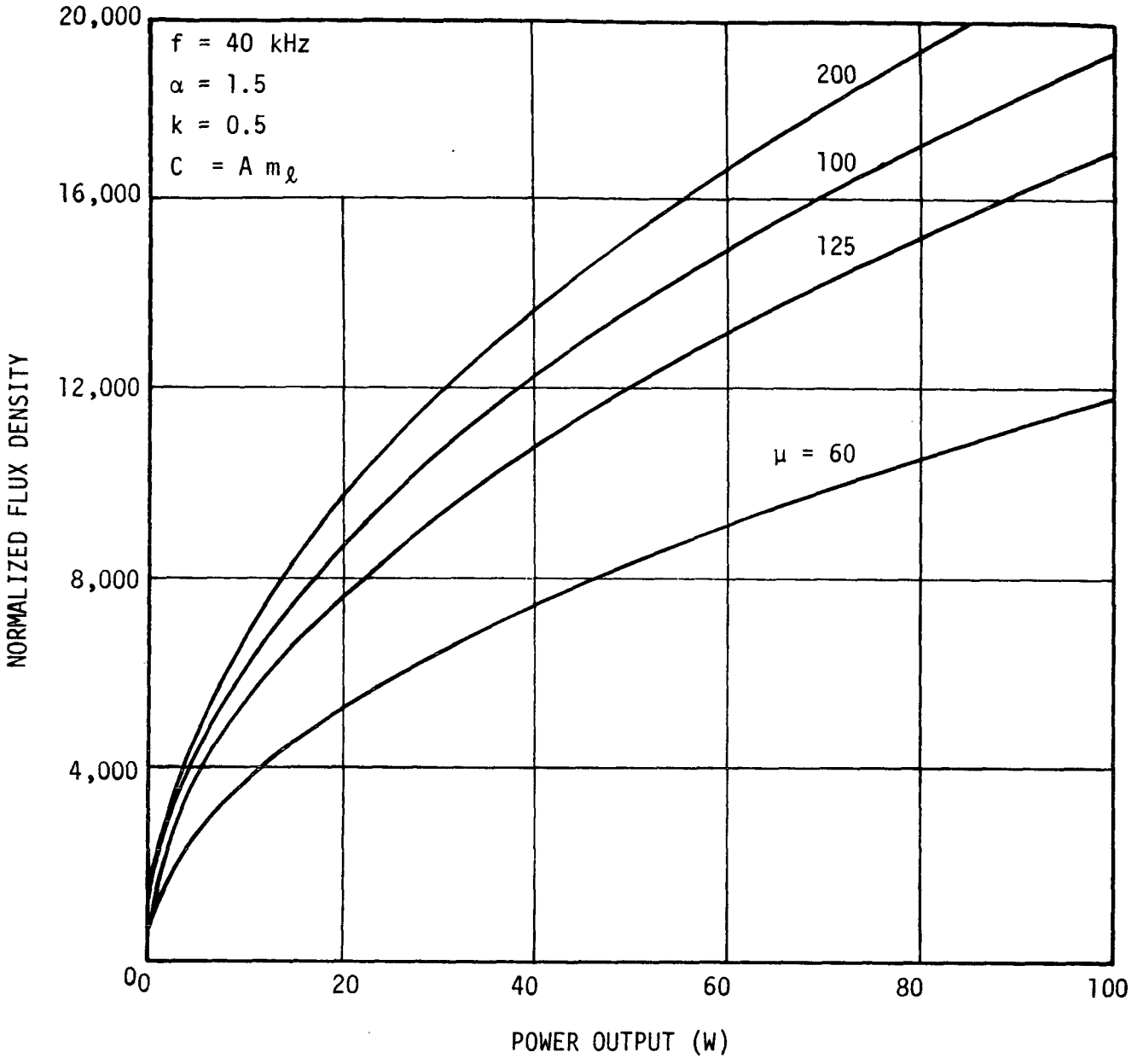


FIGURE C.8-5. POWER OUTPUT AS A FUNCTION OF NORMALIZED FLUX DENSITY

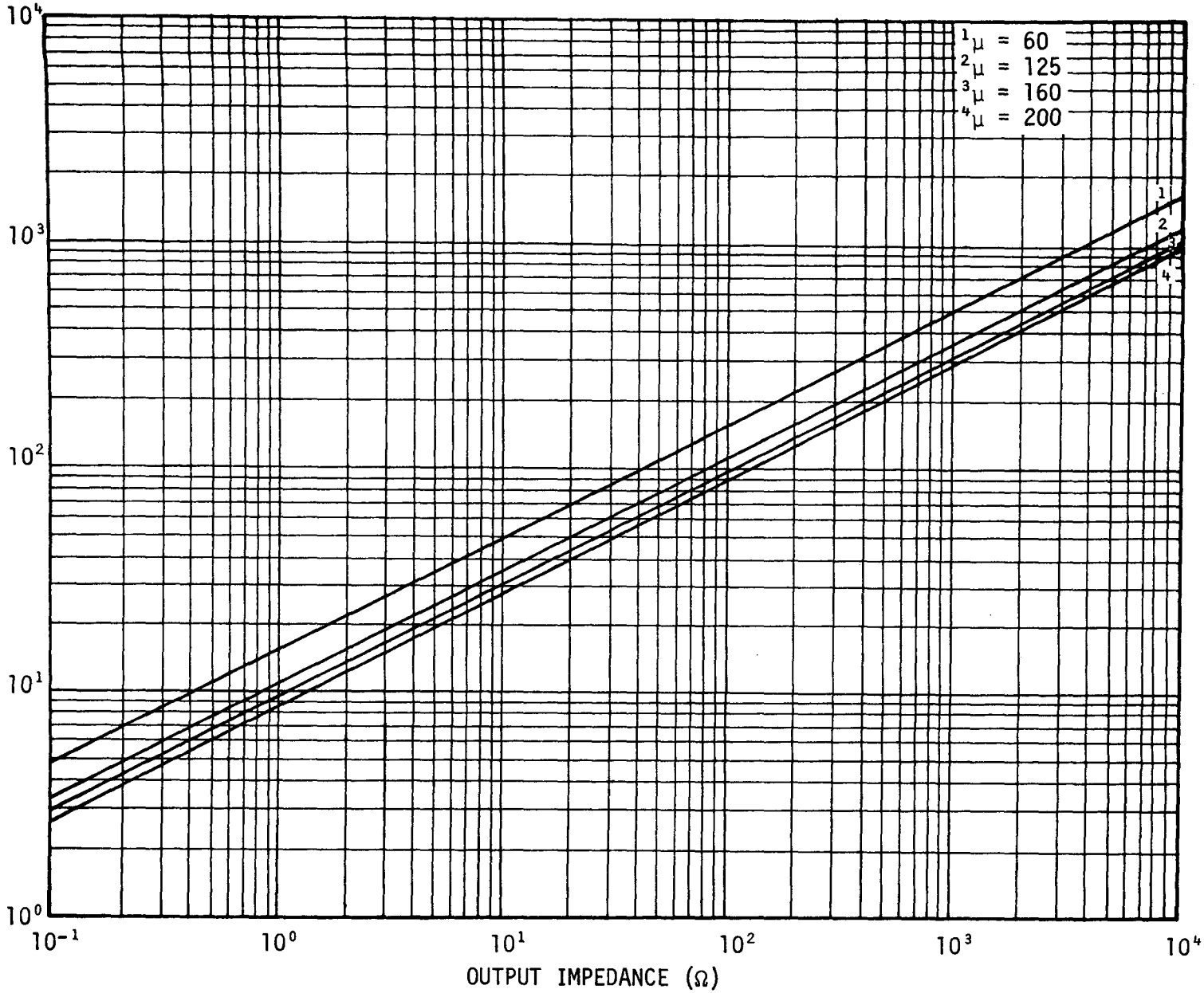


FIGURE C.8-6. OUTPUT IMPEDANCE AS A FUNCTION OF NORMALIZED NUMBER OF TURNS

C.9. ENERGY STORAGE TRADEOFF ANALYSIS

The purpose of the analysis presented here was to determine which of three possible approaches of energy storage would be optimum for use in the power supply. The three candidate approaches analyzed were a large capacitor, nickel-cadmium batteries, and an energy storage device (ESD).

C.9.1 CAPACITOR

A capacitor has the capability of storing energy and releasing this energy as a function of power and time. This energy storage capability can be related to power and time as follows.

Referring to Figure C.9-1, let V equal the input line voltage at the capacitor (C) before the switch is opened, at time t_o (representing a power drop-out), and ΔV equal the total voltage change across the capacitor (C) during the time the power has dropped out $[t - t_o]$. Also in the figure, i_L is the load current.

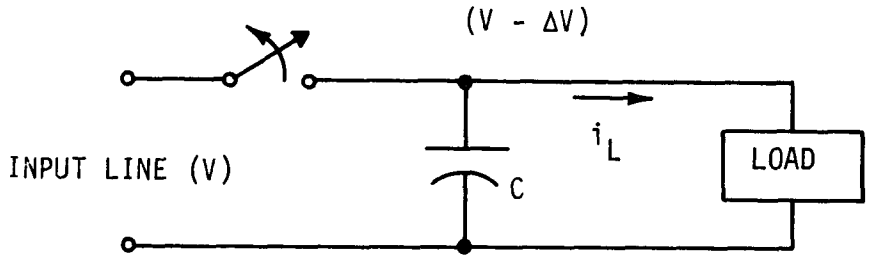


FIGURE C.9-1. SIMPLIFIED SCHEMATIC OF CAPACITOR ENERGY STORAGE ELEMENT

The energy (E) supplied to the load from the capacitor can be expressed as

$$E = \int_{t_o}^{t} \frac{P_{out}}{\eta} \, dt$$

where

P_{out} - power supply output voltage

η - efficiency of power supply

and can be related to the change in capacitor charge (Q) as

$$\int_{t_o}^{t} \frac{P_{out}}{\eta}\, dt = \int_{V}^{(V - \Delta V)} Q\, dv = \int_{V}^{(V - \Delta V)} CV\, dv .$$

Then

$$\frac{P_{out}\,[t - t_o]}{\eta} = \frac{1}{2} C\, [V^2 - (V - \Delta V)^2] .$$

Solving for the value of capacitance,

$$C = \frac{P_{out}\,[t - t_o]}{\eta\, \Delta V\, [V - \frac{\Delta V}{2}]}$$

where

C - capacitance required

$[t - t_o] = \Delta t$ - interval of time during which the power drops out

ΔV - change in voltage across the capacitor

V - input voltage just before power drop-out

P_{out} - output power of the power supply

η - efficiency of power supply .

For the proposed configuration considered, the energy storage capacitor can be placed at three different locations:

- Input to the power supply
- Input to each inverter
- At each output regulated voltage.

The line regulation requirements made considering an energy storage capacitor at each output voltage impractical. The general expression for the required capacitance at the input of the power supply for the worst-case input (90 volts) is plotted in Figure C.9-2. The tradeoff analysis was performed for a typical case (ΔV = 30V, Δt = 10 msec); however, the results can be generalized:

$$C = 700\ \mu F \begin{cases} \Delta V = 30V \\ \Delta t = 10\ \text{msec} \end{cases} \quad \text{(from Figure C.9-2)}$$

Similar calculations were made for an energy storage capacitor placed at the input of each inverter.

The cost and volume tradeoff results for the two configurations are tabulated in Table C.9-1.*

TABLE C.9-1. COST AND VOLUME TRADEOFF BETWEEN SINGLE AND MULTIPLE CAPACITORS

	COST	VOLUME
Single Capacitor at Input of the Power Supply	$ 600	45 cubic inches
Capacitor at the Input of Each dc-dc Inverter Within the Power Supply	$1000	70 cubic inches

The tradeoff analysis favors the use of a single capacitor at the input of the power supply. This also is more reliable and flexible to changes in design parameters of the supply.

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* Cost and volume data was obtained from Transistor Capacitor Co., Bennington, Vermont.

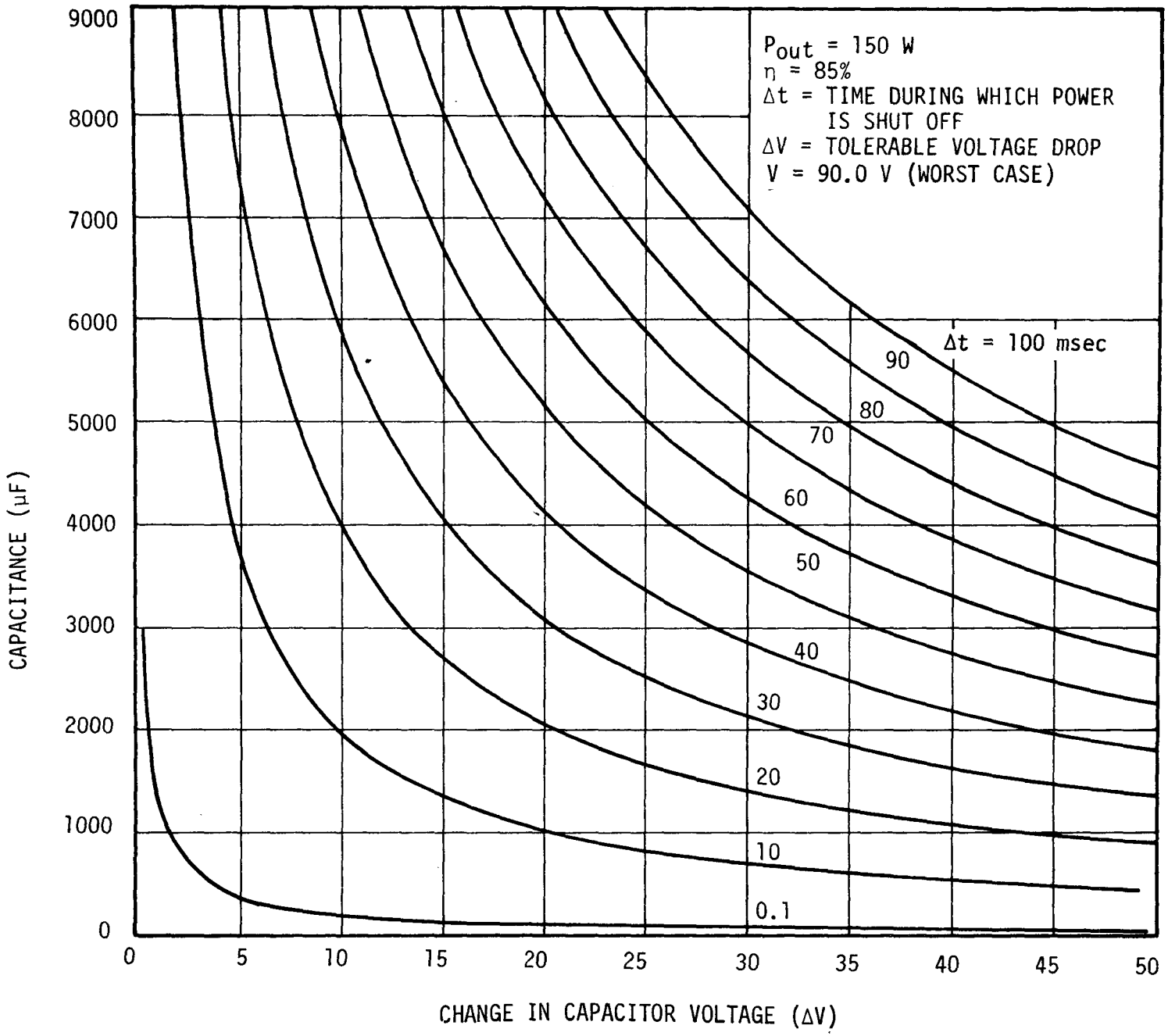

FIGURE C.9-2. ENERGY STORAGE CAPACITANCE AS A FUNCTION OF POWER DROP-OUT TIME AND CAPACITOR VOLTAGE VARIATIONS

C.9.2 ENERGY STORAGE DEVICE (ESD)

(An ESD is a recently developed energy storage component which has a very high capacitance-to-unit-volume ratio. However, based on currently available data, ESDs characteristically have a high series resistance and an extremely low voltage rating.

For example, since the typical voltage rating of an ESD is 0.5 volts and the typical series resistance is approximately 1.0 ohms, the number of cells required to obtain a voltage rating of 250 Vdc and an impedance of 0.1 ohm can be calculated as follows:

$$N = \left(\frac{\text{Voltage Required}}{\text{ESD Voltage Rating}}\right)\left(\frac{\text{ESD Impedance}}{\text{Impedance Required}}\right)$$

$$N = \left(\frac{250}{0.5}\right)\left(\frac{1.0}{0.1}\right) = 5000 \text{ cells}$$

However, a great improvement in the series resistance parameter is expected in the near future ($\approx$ 0.15 ohms). Recomputing the number of cells required,

$$N = \left(\frac{250}{0.5}\right)\left(\frac{0.15}{0.1}\right) = 750 \text{ cells}$$

The total volume required can be estimated by allowing one-third of a cubic inch per cell for a total volume of 250 in^3.

The ESD will be impractical for use in the power supply until the voltage ratings of these devices are substantially improved, which is not expected in the near future.

C.9.3 NICKEL-CADMIUM BATTERY

A battery is a very efficient way of supplying power. Calculations were performed to estimate the cost and volume of a NICAD battery

capable of providing 150 watts.* The results are

- Volume: 35 in^3
- Cost: $100.

If the approximate volume and cost of a charger, which is necessary to maintain battery charge, is considered, the total cost and volume is compatible with using a capacitor.

The major disadvantage of using NICAD batteries is their limited operational temperature range. (To keep battery efficiency above 80 percent, the operating temperature must be in the range of +10°C to +30°C.) This characteristic requires that a heater be used during low-temperature operation (below +10°C) and possibly a thermoelectric cooler at high temperatures (above +30°C). This introduces serious disadvantages in efficiency since the heater or cooler power represents a direct power loss.

The major advantage of NICAD batteries is that they are capable of providing energy for very long durations. In such a case, where power interruption is long, NICAD batteries may be the only choice possible.

C.9-4 CONCLUSIONS

The recommended energy storage element selected for this power supply was a capacitor placed at the input of the power supply. A capacitor has definite size, weight, and cost advantages over an ESD and a NICAD battery, when the cost of battery charger and peripheral circuitry is considered. However, when power interruptions with durations appreciably greater than 10 milliseconds are encountered, NICAD batteries may be the only possible choice, since they are the only device capable of providing the relatively long term energy required.

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*This data was based on utilizing NICAD battery (Part Number 500 BH) manufactured by Gould, Inc., St. Paul, Minnesota.

C.10. ANALYSIS OF THE POWER SUPPLY CONTROL LOOP

The purpose of the analysis discussed here was to derive the power supply control loop transfer function such that power supply performance could be predicted.

C.10.1 GENERAL

The performance of the power supply can be determined through an analysis of the control loop. A simplified block diagram of the control loop is shown in Figure C.10-1.

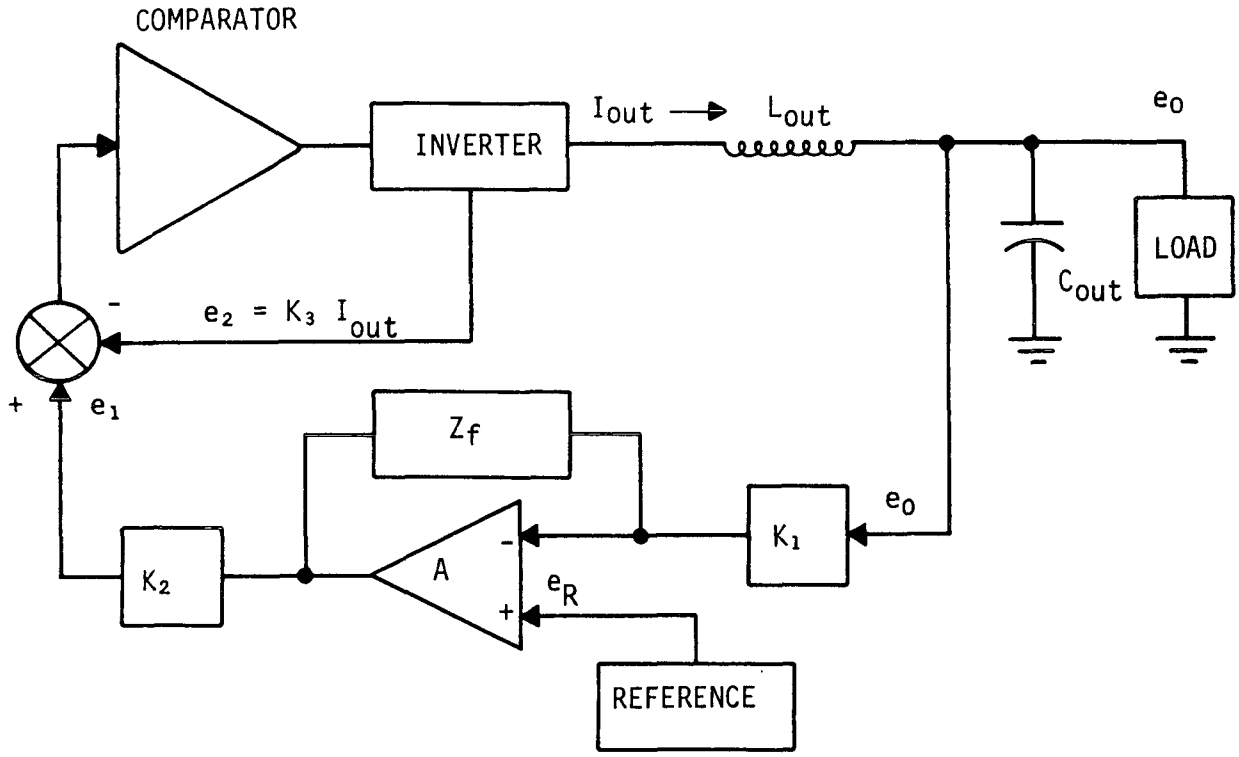


FIGURE C.10-1. SIMPLIFIED BLOCK DIAGRAM OF THE POWER SUPPLY CONTROL LOOP

C.10.2 OPEN-LOOP TRANSFER FUNCTION (GH)

The inverter-comparator module can be modeled as a voltage-programmable current source, as shown in Figure C.10-2.

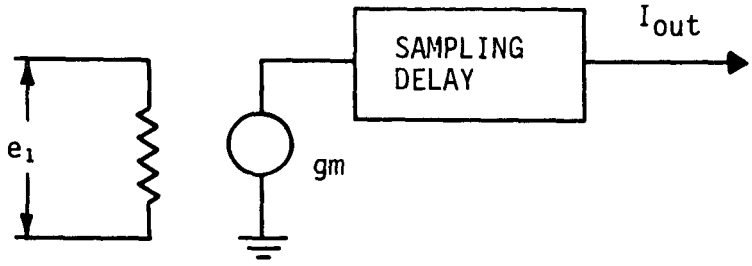


FIGURE C.10-2. INVERTER MODEL

The switching action of the inverter and the corresponding sampling of the comparator introduce a sampling delay. This delay is a phase delay of the output current and can be represented as

$$\measuredangle = \frac{\omega_f}{\omega_c} \quad (180°)$$

where

$\measuredangle$ - the delay phase angle

ω_f - the radian frequency of the feedback signal

ω_c - the radian carrier frequency, which is equal to twice the radian inverter operating frequency.

Therefore, the inverter output current can be expressed as

$$I_{out} = gm\ e_1 \underline{/\!-\left(\frac{\omega_f}{\omega_c}\right)\ 180°}$$

where

e_1 - feedback voltage

I_{out} - the inverter output current

gm - the transconductance of the inverter

$$\left(gm = \frac{\Delta I_{out}}{\Delta e_1} \propto \frac{1}{K_3}\right)$$

K_3 - constant.

Since the output current is independent of the output inductor (L_{out}), the output voltage (e_o) may be expressed as

$$e_o = (I_{out})\,(Z_{out})$$

where the output impedance (Z_{out}) equals the load impedance (R_L) shunted by the impedance of the capacitor (C_{out}).

$$Z_{out} = \frac{R_L}{S\,R_L\,C_{out} + 1}$$

and, therefore,

$$e_o = \frac{I_{out}\,R_L}{S\,R_L\,C_{out} + 1} = \frac{gm\,e_1 \left| -\frac{\omega_f}{\omega_c}\,(180°)\right. \quad R_L}{S\,R_L\,C_{out} + 1}$$

The equation defining the feedback voltage (e_1) is

$$e_1 = K_2 \left(\frac{Z_f}{K_1}\right)\,(e_R - e_o)$$

where

K_2 - the gain of the input-to-output isolator, volts/volt

Z_f - feedback compensation network impedance

K_1 - output voltage sense resistance

e_R - reference voltage.

The open-loop transfer function (GH) may therefore be expressed as

$$G(\omega)\, H(\omega) = \frac{e_o}{e_R - e_o} = \left(gm \left| -\frac{\omega_f}{\omega_c} (180°)\right)\right)\left(\frac{R_L}{S\, R_L\, C_{out} + 1}\right) \times \left[K_2\left(\frac{Z_f}{K_1}\right)\right]$$

Since for any output voltage the transconductance (gm), load resistance (R_L), and the voltage sense resistance (K_1) can be defined in terms of the output voltage as

$$gm = \frac{K_4}{e_o}$$

$$K_1 = K_5\, e_o$$

$$R_L = \frac{e_o^2}{P_{out}}$$

where

K_2, K_4, K_5 - constants

e_o - output voltage

P_{out} - output power

then

$$gm\left(\frac{K_2}{K_1}\right) R_L = \left(\frac{K_4}{e_o}\right)\left(\frac{1}{K_5\, e_o}\right)\left(\frac{e_o^2}{P_{out}}\right) = \frac{K_6}{P_{out}}$$

where

$$K_6 = \frac{K_2\, K_4}{K_5} = \text{constant}$$

and the equation representing GH reduces to

$$G(\omega)\, H(\omega) = K_6 \left| -\frac{\omega_f}{\omega_c}\,(180°) \right. \left(\frac{1}{S\, R_L\, C_{out} + 1}\right) (Z_f) \left(\frac{1}{P_{out}}\right).$$

Note that the magnitude and phase of GH are independent of output voltage and dependent on output current only.

C.10.3 LOAD REGULATION

The load regulation, or the change in output voltage due to a change in output current, can be defined in terms of the output impedance (Z_{out}).

If

$$\text{Load Regulation} = \frac{\Delta e_o}{\Delta I_{load}}\ (100\%)$$

then,

$$\text{Load Regulation} = Z'_{out}\ (100\%).$$

Since

$$Z_{out} = \frac{R_L}{S\, R_L\, C_{out} + 1}$$

then

$$Z'_{out} = \frac{\left(\dfrac{R_L}{S\, R_L\, C_{out} + 1}\right)}{G(\omega)\, H(\omega)}\ .$$

The output impedance depends on frequency. The load regulation may be determined by letting the radian frequency (ω) equal zero as:

$$\text{Load Regulation} = \frac{R_L}{G(o)\, H(o)} \times 100\%.$$

The output impedance $Z'_{out}(\omega)$ shows the dynamic regulation.

C.10.4 LINE REGULATION

The line regulation of the selected power supply design is inherently good. The regulator is essentially a current source and a true current source is not affected by voltage changes.

To predict line regulation, a close inspection of the control circuit must be made. The first fact that must be determined is, if the feedback voltage (e_1) is made constant and the input voltage is increased, how does the average output current ($I_{out\ AV}$) change?

Since the rate of change of output current is determined by L_{out}, as

$$\frac{I_{out\ (t)}}{dt} = \frac{E_{in}\ N_R - E_{out}}{L_{out}}$$

where

E_{in} - input voltage

N_R - transformer turn ratio

E_{out} - output voltage

L_{out} - output filter inductance

the rate of change of output current increases with increased voltage.

Since the rate of change of current has changed and the comparator has a finite bandwidth and therefore a finite rise time and delay time, the current peak at which the inverter is cut off changes. This is shown in Figure C.10-3.

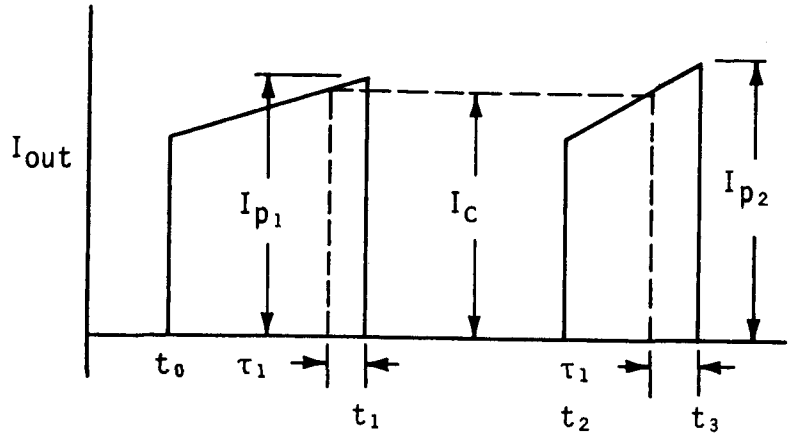


FIGURE C.10-3. PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

In this figure, shown as an example, at time t_o to t_1 the input voltage equals E_1 and at time t_2 to t_3 the input voltage is $2(E_1)$. This is shown by the slope of the pulse occurring at t_2 being twice that of the pulse occurring at t_0. Since the delay and rise time of the comparator (τ) does not change, the current I_{p_2} is larger than I_{p_1}. This peak current may be related as follows

$$I_{p_1} = I_c + \frac{\left(E_{in} N_R - E_{out}\right)\tau}{L_{out}}$$

$$I_{p_2} = I_c + \frac{\left(E_{in} N_R - E_{out}\right)\tau}{L_{out}}$$

where I_C is the threshold current level of the comparator.

The following equations may be used to calculate the resultant change in output voltage ($E_2 - E_1$).

Since

$$\frac{P_{in}}{\eta} = P_{out}$$

(where η is the efficiency of the power supply) and

$$\frac{E_{in}\, I_{in}}{\eta} = P_{out}$$

then

$$P_{out_1} = \frac{E_{in_1}}{\eta} \int_{t_o}^{t_1} I_{in}(t)\, dt$$

$$P_{out_2} = \frac{E_{in_2}}{\eta} \int_{t_2}^{t_3} I_{in}(t)\, dt$$

Also, since

$$E_{out} = (P_{out}\ R_L)^{\frac{1}{2}}$$

then

$$\Delta E_{out} = (P_{out_2}\ R_L - P_{out_2}\ R_L)^{\frac{1}{2}}$$

This is the output voltage change without feedback. To obtain the line regulation, this result must be divided by $G(\omega)\ H(\omega)$; this provides the closed-loop line regulation as

$$\Delta E_{out} = \frac{(P_{out_1} R_L - P_{out_2} R_L)^{\frac{1}{2}}}{G(\omega)\ H(\omega)}$$

APPENDIX D. BREADBOARD RESULTS

D.1 INTRODUCTION

Concurrent with Phases II and III of this study, a breadboard of a single regulator was constructed. This effort was undertaken to verify the analysis and predicted performance of the power supply, which was determined during Phase II, and to authenticate the circuit such that the efforts of Phases III and IV of the study could be supported by actual test data.

An output power of 50 watts and a voltage level of 5.0 volts were selected for this breadboard. These output levels were chosen because they represent the most difficult levels under which the regulator must operate, when both the required performance and packaging are considered. The following sections summarize the data received from the breadboard.

D.2 BREADBOARD STATIC PERFORMANCE

Two regulators were used in the breadboard. The first regulator used a conventional output power rectifier (a diode with a forward voltage drop greater than 0.7 volt) and a conventional power switching transistor (a transistor with switching times four to five times those of the specified transistor). The second regulator utilized a conventional power switching transistor and a Schottky barrier diode in place of the conventional output power rectifier. These diodes have a substantially lower forward voltage drop (0.35 volt) and therefore improve the efficiency measurements of this regulator over those for the first regulator considered.*

*It must be noted that these regulators are identical in configuration, consistent with Figure D-4, and differ only in the type of output rectifier utilized as indicated above.

A number of data points representing the static performance of the regulators were recorded. The data points were taken for this regulator using the conventional output rectifier when the input voltage was varied from 80 to 120 volts. Voltages of 80 and 120 volts were used for the second regulator. This data is tabulated in Tables D-1 through D-6.

Figure D-1 shows the efficiency of the power supply (with the conventional output rectifiers) as a function of the output power level. Figure D-2 shows the same data when Schottky barrier diodes are used for the rectifiers. As indicated by a comparison of the figures for the two regulators, the Schottky barrier diodes used in the second regulator substantially improve the efficiency measurements of this regulator over those for the regulator using the conventional output rectifier.

D.3 REGULATOR WAVEFORMS

Figure D-3 shows the waveforms recorded (photographed) from the regulator in operation. These waveforms are included to aid the reader in understanding the operation of the regulator. Waveforms representing the dynamic performance of the regulator are shown in Figure D-5.

D.4 POWER SUPPLY PERFORMANCE CHARACTERISTICS

A summary of the recorded performance characteristics of the power supply is shown in Table D-7.

TABLE D-1. STATIC PERFORMANCE DATA FOR THE REGULATOR USING A CONVENTIONAL OUTPUT POWER RECTIFIER WHEN THE INPUT VOLTAGE IS 80 VOLTS

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (amp)	INPUT CURRENT (mA)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY (%)
4.981	0.00	42.40	3.390		
4.981	0.494	44.50	3.560	2.460	69.118
4.981	0.982	77.44	6.195	4.891	78.953
4.981	2.430	181.60	14.528	12.103	83.313
4.981	4.850	361.70	28.936	24.157	83.487
4.981	7.200	545.30	43.624	35.863	82.209
4.981	9.600	733.80	58.704	47.817	81.455
4.981	10.060	771.30	61.704	50.108	81.208

TABLE D-2. STATIC PERFORMANCE DATA FOR THE REGULATOR USING A CONVENTIONAL OUTPUT POWER RECTIFIER WHEN THE INPUT VOLTAGE IS 90 VOLTS

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (amp)	INPUT CURRENT (mA)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY (%)
4.981	0.0	38.90	3.501		
4.981	0.494	41.12	3.700	2.460	66.488
4.981	0.985	70.47	6.342	4.906	77.358
4.981	2.432	163.10	14.679	12.113	82.524
4.981	4.850	323.30	29.097	24.157	83.025
4.981	7.200	487.00	43.830	35.863	81.823
4.981	9.570	654.30	58.887	47.668	80.948
4.981	10.020	690.30	62.127	49.909	80.334

TABLE D-3. STATIC PERFORMANCE DATA FOR THE REGULATOR USING A CONVENTIONAL OUTPUT POWER RECTIFIER WHEN THE INPUT VOLTAGE IS 100 VOLTS

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (amp)	INPUT CURRENT (mA)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY (%)
4.981	0.0	36.20	3.620	0.0	0.0
4.981	0.495	39.40	3.940	2.465	68.110
4.981	0.985	64.82	6.482	4.906	75.691
4.981	2.433	148.00	14.800	12.118	81.883
4.981	4.860	292.40	29.240	24.207	82.789
4.981	7.200	440.30	44.030	35.863	81.451
4.981	9.570	589.50	58.950	47.668	80.862
4.981	10.020	619.70	61.970	49.909	80.538

TABLE D-4. STATIC PERFORMANCE DATA FOR THE REGULATOR USING A CONVENTIONAL OUTPUT POWER RECTIFIER WHEN THE INPUT VOLTAGE IS 120 VOLTS

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (amp)	INPUT CURRENT (mA)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY (%)
4.981	0.0	36.40	4.368	0.0	0.0
4.981	0.495	33.90	4.068	2.465	60.609
4.981	0.983	56.80	6.816	4.896	71.835
4.981	2.433	126.20	15.144	12.118	80.023
4.981	4.860	246.60	29.592	24.207	81.804
4.981	7.200	368.70	44.244	35.863	81.057
4.981	9.570	497.30	59.676	47.668	79.878
4.981	10.020	523.00	62.760	49.909	79.524

TABLE D-5. STATIC PERFORMANCE DATA FOR THE REGULATOR USING A CONVENTIONAL POWER SWITCHING TRANSISTOR WHEN THE INPUT VOLTAGE IS 80 VOLTS

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (amp)	INPUT CURRENT (mA)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY (%)
4.983	0.0	23.0	1.840	0.0	0.0
4.982	0.117	15.40	1.232	0.582	47.312
4.983	0.334	29.10	2.328	1.664	71.491
4.984	0.495	40.50	3.240	2.467	76.144
4.987	2.435	171.60	13.728	12.143	88.456
4.991	4.850	341.30	27.304	24.206	88.654
4.995	7.200	513.60	41.088	35.964	87.529
5.015	9.550	692.00	55.360	47.893	86.512
5.016	10.000	728.90	58.312	50.160	86.020

NOTE: The change in output voltage caused by changes in load is not representative of load regulation. This change is caused primarily by line (IR) drops between the output power bus (where output voltage measurements were made) and the load (the point at which output voltage sensing was implemented).

TABLE D-6. STATIC PERFORMANCE DATA FOR THE REGULATOR USING A CONVENTIONAL POWER SWITCHING TRANSISTOR WHEN THE INPUT VOLTAGE IS 120 VOLTS

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (amp)	INPUT CURRENT (mA)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY (%)
	0.0	13.30	1.596	0.0	0.0
4.983	0.334	26.20	3.144	1.664	52.936
4.984	0.495	35.00	4.200	2.467	58.740
4.987	2.435	123.00	14.760	12.143	82.271
4.991	4.850	236.00	28.320	24.206	85.474
4.995	7.200	351.00	42.120	35.964	85.384
4.999	9.650	483.00	57.960	48.240	83.230
5.000	10.100	50.40	60.480	50.500	83.498

TABLE D-7. POWER SUPPLY PERFORMANCE CHARACTERISTICS

ITEM	DATA
Efficiency	86%[1]
Line Regulation	< 0.02%
Load Regulation	< 0.02%
Output Ripple and Noise	25 mV p-p
Input Ripple and Noise	6 mA p-p[2]
Worst-Case Step Load Transient	1.2 V [3]

NOTES:

[1]Measured at full load, 80-volt input

[2]Without input EMI filter

[3]No load to full load (settling time 1.0 msec)

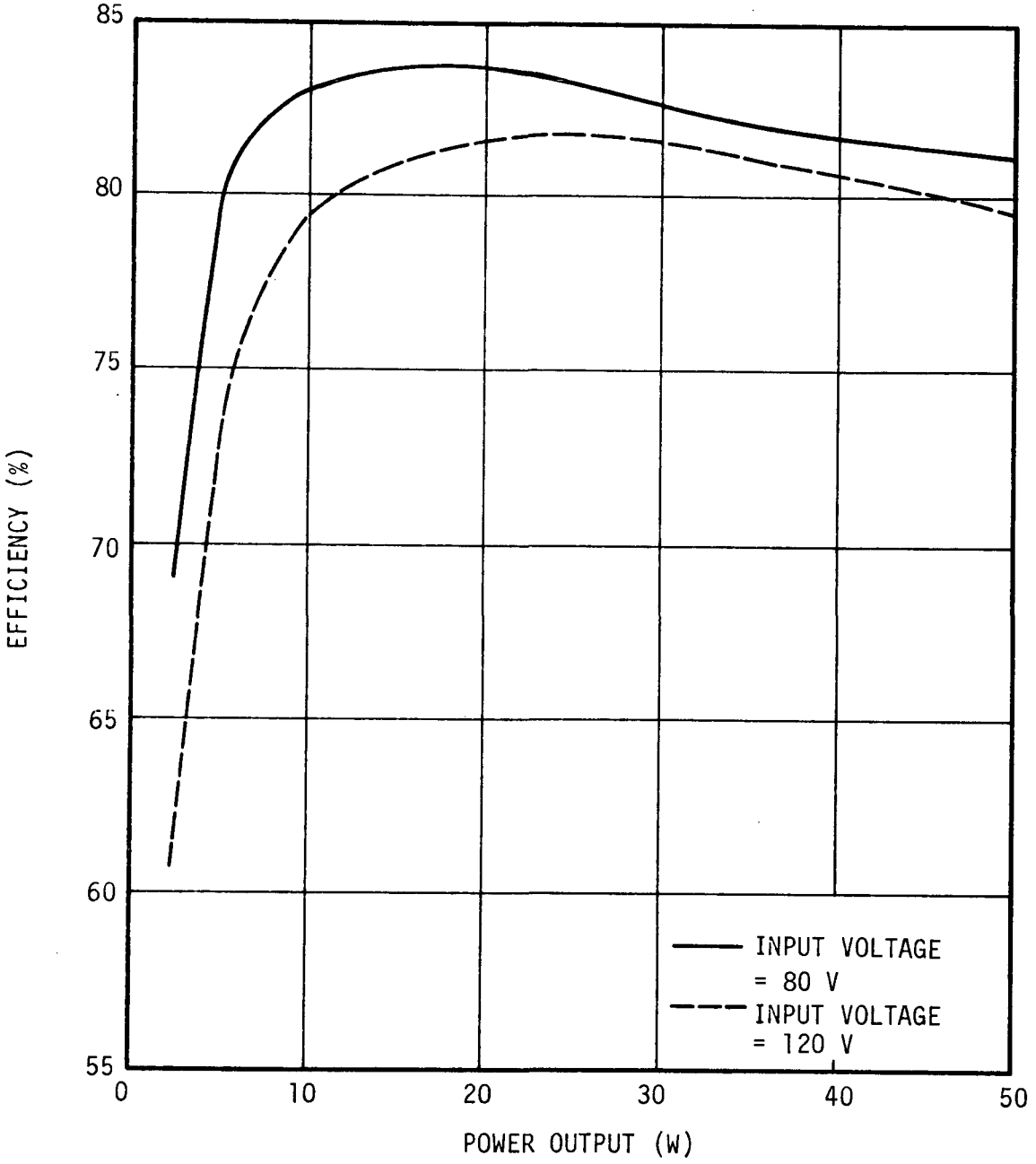


FIGURE D-1. EFFICIENCY AS A FUNCTION OF OUTPUT POWER LEVEL FOR THE REGULATOR USING A CONVENTIONAL OUTPUT POWER RECTIFIER

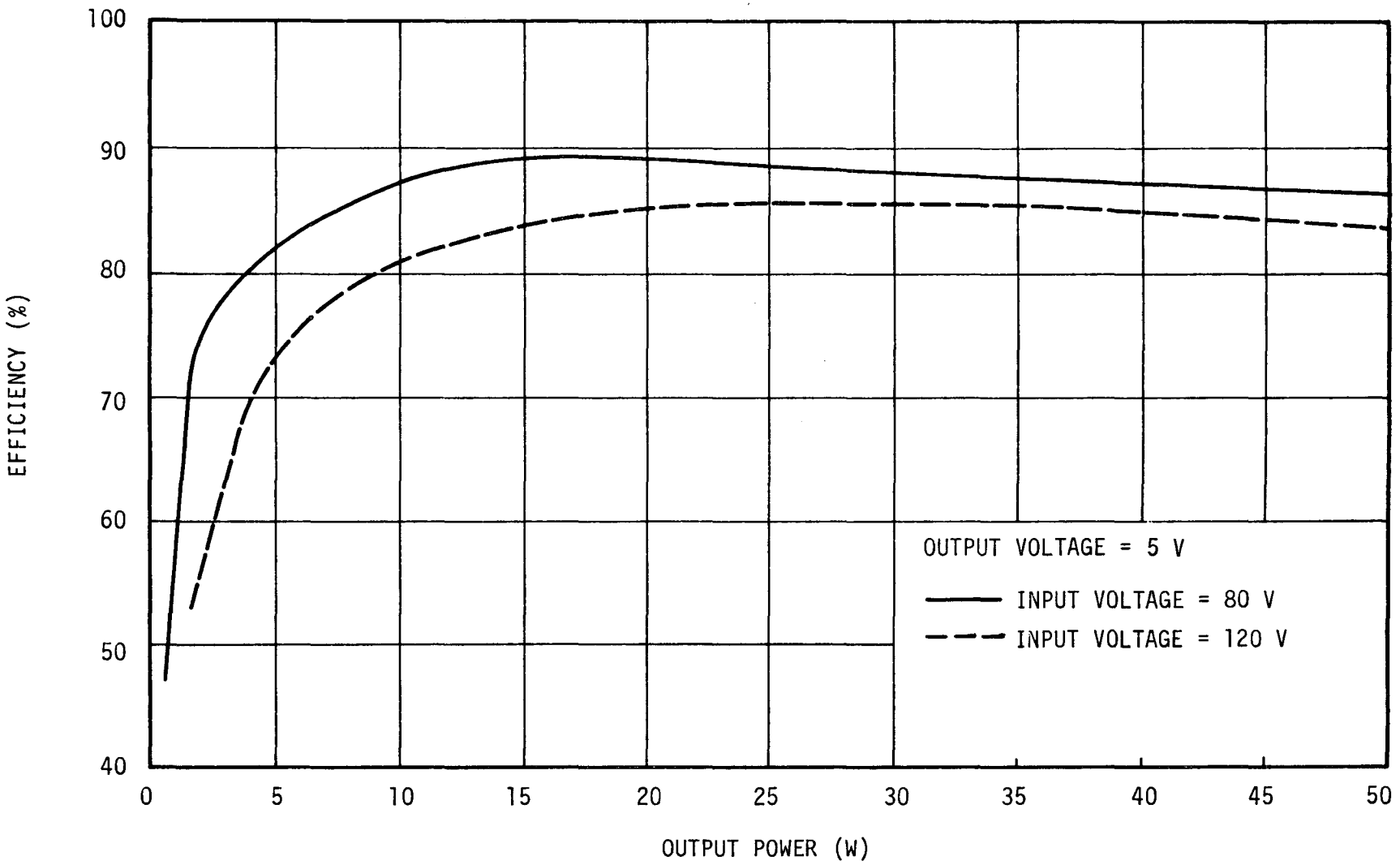
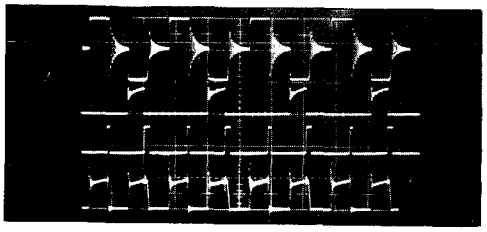
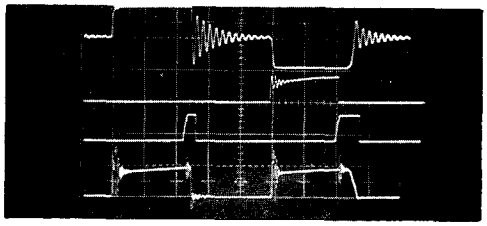


FIGURE D-2. EFFICIENCY AS A FUNCTION OF OUTPUT POWER LEVEL FOR THE REGULATOR USING A CONVENTIONAL POWER SWITCHING TRANSISTOR



TIME (20 μsec/cm)



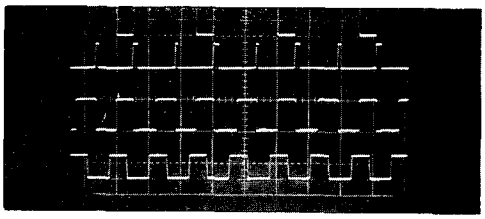
TIME (5 μsec/cm)

a. COLLECTOR VOLTAGE WAVEFORM OF THE INVERTER POWER TRANSISTOR AT 100 V/cm (Q7 OF THE REGULATOR, PREDRIVER, AND DRIVER HYBRID SHOWN IN FIGURE D-4)

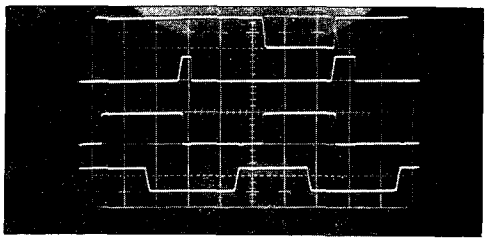
b. COLLECTOR VOLTAGE WAVEFORM OF THE PREDRIVE TRANSISTOR, 20 V/cm (Q5 OF THE REGULATOR, PREDRIVER, AND DRIVER HYBRID SHOWN IN FIGURE D-4)

c. COMPARATOR OUTPUT VOLTAGE WAVEFORM, 10 V/cm (PIN 9 OF THE PREREGULATOR AND COMPARATOR HYBRID SHOWN IN FIGURE D-4)

d. COMPARATOR INPUT VOLTAGE WAVEFORM (REPRESENTS PRIMARY CURRENT), 100 mV/cm (PIN 8 OF THE PREREGULATOR AND COMPARATOR HYBRID SHOWN IN FIGURE D-4)



TIME (20 μsec/cm)



TIME (5 μsec/cm)

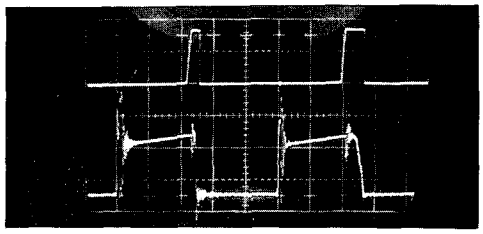
a. CONTROL LOGIC OUTPUT DRIVE VOLTAGE WAVEFORM, 10 V/cm (PIN 2 OF THE OSCILLATOR AND CONTROL LOGIC HYBRID SHOWN IN FIGURE D-4)

b. COMPARATOR OUTPUT VOLTAGE WAVEFORM, 20 V/cm (PIN 9 OF THE PREREGULATOR AND COMPARATOR HYBRID SHOWN IN FIGURE D-4)

c. OUTPUT VOLTAGE WAVEFORM AT THE OUTPUT OF THE MEMORY FLIP-FLOP, 10 V/cm [THE "Q" OUTPUT OF FLIP FLOP IC3(b) IN THE OSCILLATOR AND CONTROL LOGIC HYBRID SHOWN IN FIGURE D-4)

d. OSCILLATOR OUTPUT VOLTAGE WAVEFORM, 10 V/cm (PIN 9 OF THE OSCILLATOR AND CONTROL LOGIC HYBRID SHOWN IN FIGURE D-4)

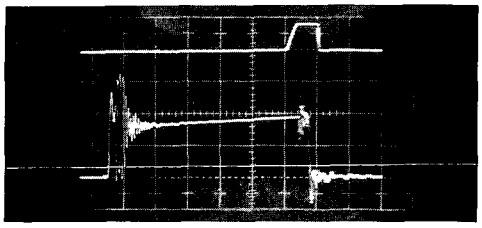
FIGURE D-3. WAVEFORMS OF REGULATOR IN OPERATION



a

b

TIME (5 μsec/cm)



a

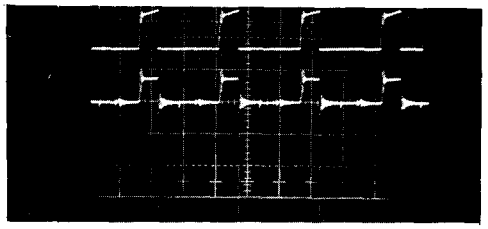
b

TIME (2 μsec/cm)

a. COMPARATOR OUTPUT VOLTAGE WAVEFORM, 5 V/cm IN TOP FIGURE/ 10 V/cm IN LOWER FIGURE (PIN 9 OF PREREGULATOR AND COMPARATOR HYBRID SHOWN IN FIGURE D-4)

b. COMPARATOR INPUT VOLTAGE WAVEFORM REPRESENTING PRIMARY LOAD CURRENT, 60 mV/div (MEASURED ACROSS EXTERNAL RESISTOR R1 IN FIGURE D-4)

FIGURE D-3. - Continued



a

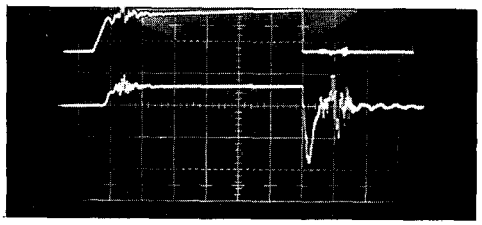
b

TIME (20 μsec/cm)
ONE-HALF LOAD

a

b

TIME (1 μsec/cm)
ONE-HALF LOAD



a

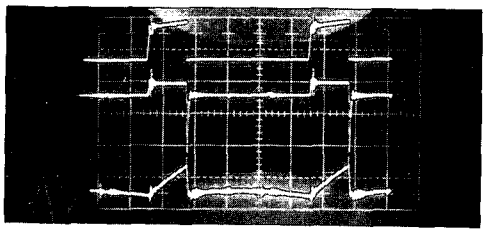
b

TIME (1 μsec/cm)
FULL LOAD

a. COLLECTOR VOLTAGE WAVEFORM OF THE PREDRIVE TRANSISTOR, 10 V/cm (Q5 OF THE REGULATOR AND PRE-DRIVER AND DRIVER HYBRID SHOWN IN FIGURE D-4)

b. INVERTER POWER TRANSISTOR BASE CURRENT WAVEFORM, 100 mA/cm IN THE TOP TWO FIGURES/200 mA/cm IN THE BOTTOM FIGURE (Q7 OF THE REGULATOR AND PRE-REGULATOR HYBRID SHOWN IN FIGURE D-4)

FIGURE D-3. - Continued

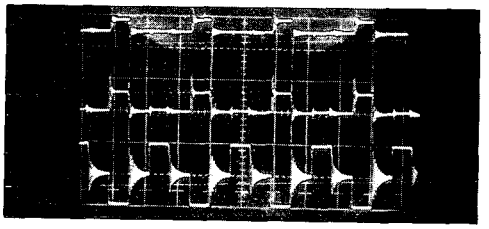


TIME (20 μsec/cm)
FULL LOAD

a. COLLECTOR VOLTAGE WAVEFORM OF THE PREDRIVE TRANSISTOR, 10 V/cm (Q5 OF THE REGULATOR, PREDRIVER, AND DRIVER HYBRID SHOWN IN FIGURE D-4)

b. INVERTER POWER TRANSISTOR BASE CURRENT WAVEFORM, 200 mA/cm (Q7 OF THE REGULATOR, PREDRIVER, AND DRIVER HYBRID SHOWN IN FIGURE D-4)

c. VOLTAGE WAVEFORM ACROSS PREDRIVER CIRCUIT CAPACITOR (EXTERNAL CAPACITOR C2 IN FIGURE D-4)

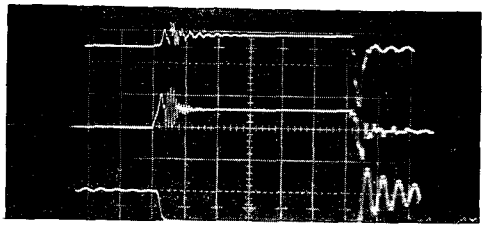


TIME (20 μsec/cm)
FULL LOAD

a. INVERTER POWER SWITCH BASE CURRENT WAVEFORM, 200 mA/cm

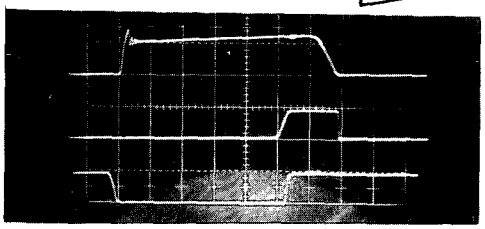
b. INVERTER POWER SWITCH BASE TO EMITTER VOLTAGE WAVEFORM, 2.0 V/cm

c. INVERTER POWER SWITCH COLLECTOR VOLTAGE WAVEFORM, 100 V/cm



TIME (1 μsec/cm)
FULL LOAD

FIGURE D-3. - Continued

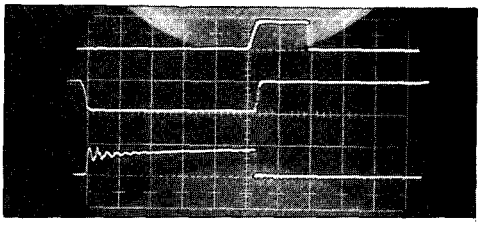


TIME (1 μsec/cm)

a. INVERTER POWER SWITCH COLLECTOR CURRENT WAVEFORM, 0.5 A/cm

b. COMPARATOR OUTPUT VOLTAGE WAVEFORM, 10 V/cm

c. LOGIC OUTPUT DRIVE SIGNAL WAVEFORM, 20 V/cm



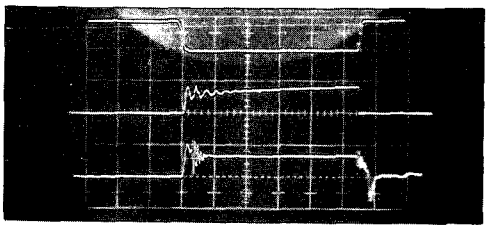
TIME (1 μsec/cm)

a. COMPARATOR OUTPUT VOLTAGE WAVEFORM, 10 V/cm

b. LOGIC OUTPUT DRIVE SIGNAL WAVEFORM, 10 V/cm

c. COLLECTOR VOLTAGE WAVEFORM OF THE PREDRIVE TRANSISTOR, 20 V/cm

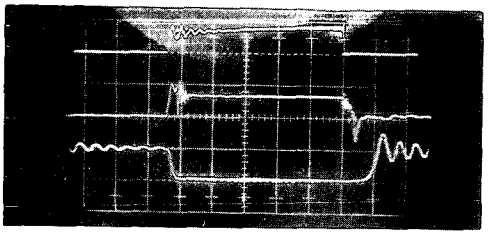
FIGURE D-3. - Continued



a. LOGIC CONTROL DRIVE SIGNAL WAVEFORM, 10 V/cm

b. COLLECTOR VOLTAGE WAVEFORM OF THE PREDRIVE TRANSISTOR, 20 V/cm

c. INVERTER POWER SWITCH BASE TO EMITTER VOLTAGE WAVEFORM, 2 V/cm



a. COLLECTOR VOLTAGE WAVEFORM OF THE PREDRIVE TRANSISTOR, 20 V/cm

b. INVERTER POWER SWITCH BASE VOLTAGE WAVEFORM, 2 V/cm

c. INVERTER POWER SWITCH COLLECTOR VOLTAGE WAVEFORM, 100 V/cm

FIGURE D-3. - Concluded

F

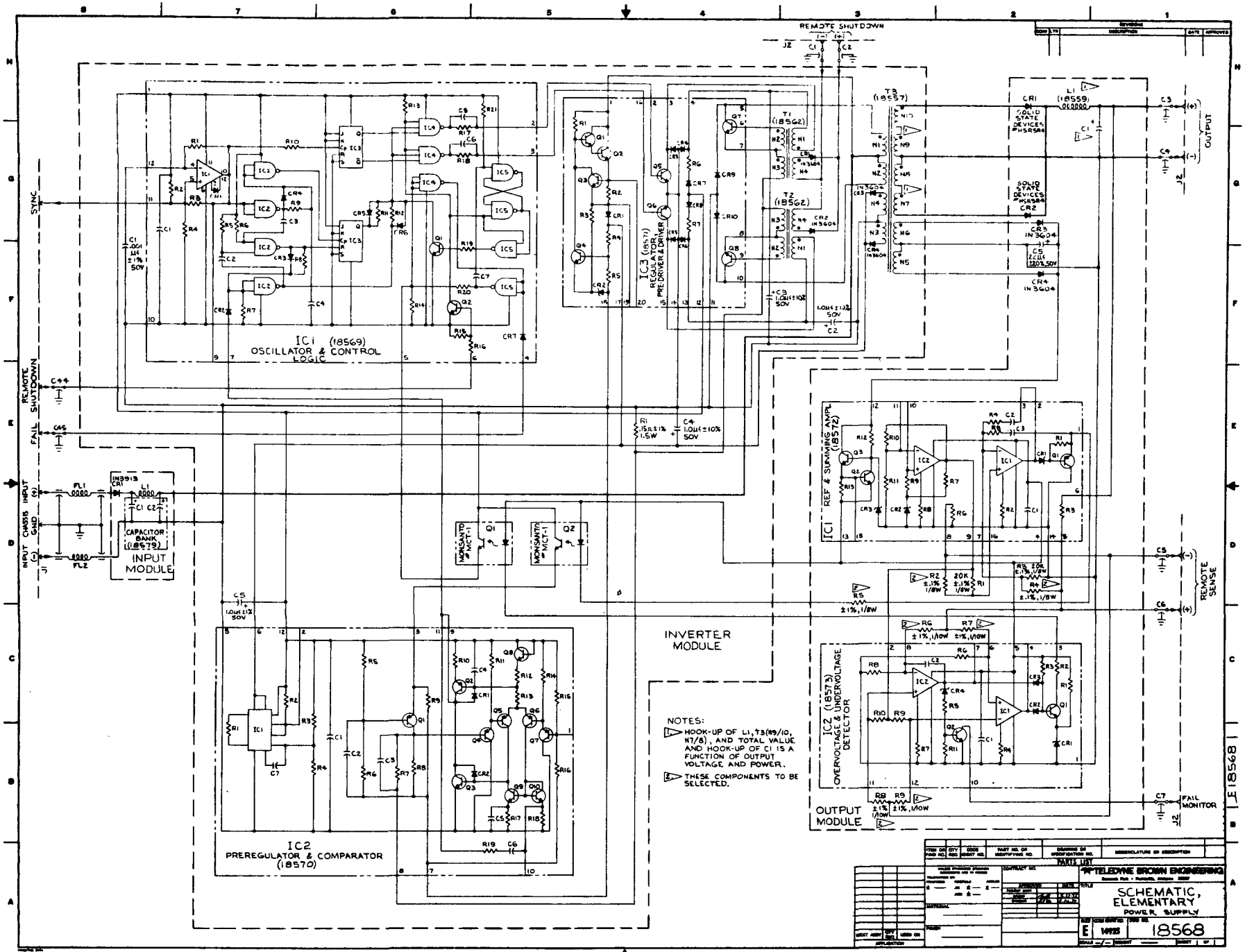
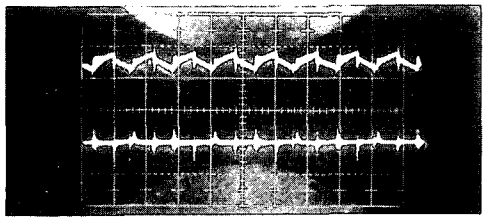


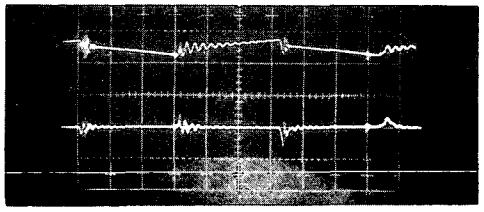
FIGURE D-4. OVERALL SCHEMATIC DIAGRAM



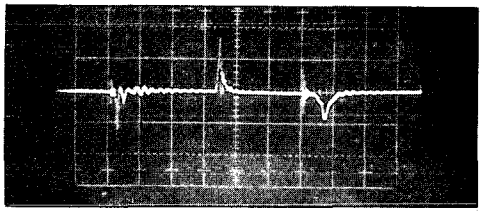
TIME (20 μsec/cm)
ONE-HALF LOAD

a. RIPPLE VOLTAGE WAVEFORM ACROS INPUT FILTER CAPACITOR, 20 mV/cm (CAPACITOR C2 IN THE INPUT MODULE SHOWN IN FIGURE D-4)

b. INPUT POWER LINE RIPPLE CURRENT WAVEFORM, 5 mA/cm



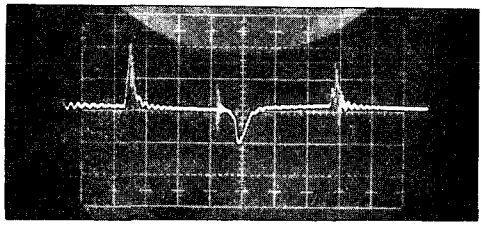
TIME (2 μsec/cm)
ONE-HALF LOAD



TIME (2 μsec/cm)

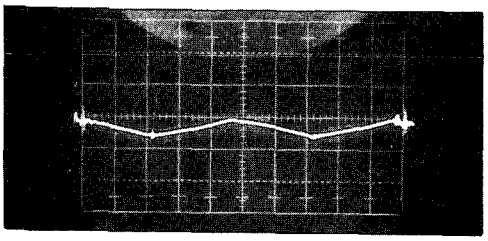
a. INPUT POWER LINE RIPPLE CURRENT WAVEFORM, ONE-HALF LOAD, 2 mA/cm

b. INPUT POWER LINE RIPPLE CURRENT WAVEFORM, FULL LOAD, 2 mA/cm



TIME (2 μsec/cm)

FIGURE D-5. WAVEFORMS OF REGULATOR DYNAMIC PERFORMANCE



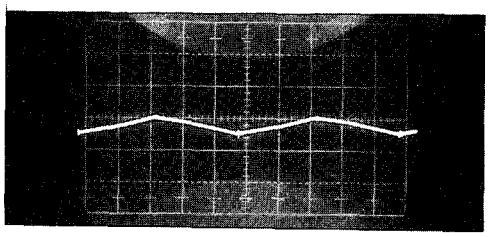
a

TIME (5 μsec/cm)

OUTPUT RIPPLE VOLTAGE WAVEFORM

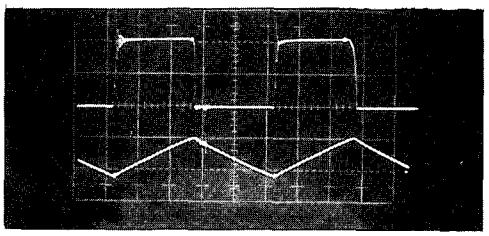
a. OUTPUT RIPPLE VOLTAGE WAVEFORM, FULL LOAD, 50 mV/cm

b. OUTPUT RIPPLE VOLTAGE WAVEFORM, ONE-QUARTER LOAD, 50 mV/cm



b

TIME (5 μsec/cm)



a

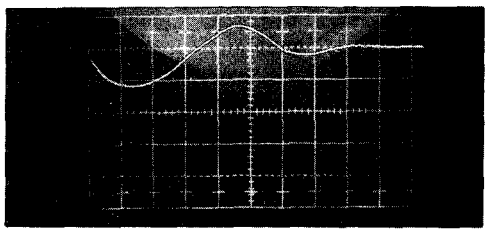
b

TIME (5 μsec/cm)

a. RECTIFIED POWER TRANSFORMER OUTPUT VOLTAGE WAVEFORM, 5 V/cm

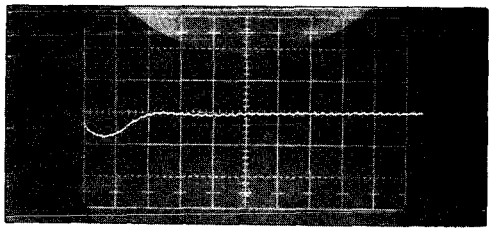
b. CURRENT WAVEFORM THROUGH THE OUTPUT INDUCTOR [L1 IN THE OUTPUT MODULE OF FIGURE D-4), 0.5 A/cm]

FIGURE D-5. - Continued



TIME (100 μsec/cm)

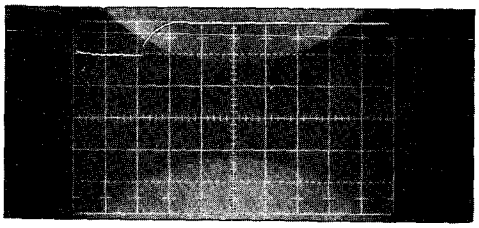
NO LOAD TO FULL LOAD OUTPUT
VOLTAGE TRANSIENT, 1.0 V/cm



TIME (100 μsec/cm)

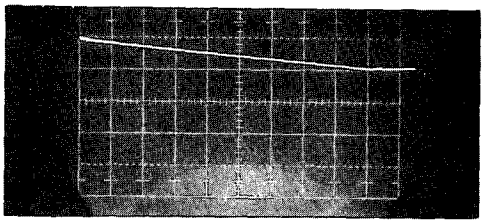
ONE-HALF LOAD TO FULL LOAD OUTPUT
VOLTAGE TRANSIENT, 0.5 V/cm

FIGURE D-5. - Continued

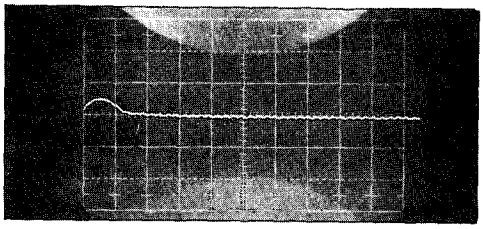


TIME (100 μsec/cm)

FULL LOAD TO NO LOAD OUTPUT VOLTAGE TRANSIENT, 1.0 V/cm (1.8 KΩ STATIC LOAD)



TIME (10 msec/cm)



TIME (100 μsec/cm)

FULL LOAD TO ONE-HALF LOAD OUTPUT VOLTAGE TRANSIENT, 0.5 V/cm

FIGURE D-5. - Concluded